ECDR-GC814-FERMI
USER MANUAL

Revision 1.0

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About This Manual describes the contents of each chapter, and provides document conventions and technical support information.

Chapters Overview

About This Manual – Describes each chapter in this users manual and provides technical support information.

Chapter 1 Introduction – Provides a general overview of the ECDR-GC814, lists the product models available, and describes operating modes and product applications

Chapter 2 Product Overview – Provides additional product information including analog signal inputs, clocking, channel configurations, and analog-to-digital data.

Chapter 3 Specifications – Provides general and environmental specifications, and power requirements for the ECDR-GC814 board.

Chapter 4 Installation and Setup - Provides board installation and setup information, including setting switches and connectors.

Chapter 5 Operating Guide – Provides information for connecting inputs to signal sources, configuring the VME Bus and the GC4016s, and synchronizing operation and control. This chapter also includes examples of data collection.

Chapter 6 Register Maps – Provides memory maps and registers for the ECDR-GC814 board.

Applicable Documents

The following sources provide important reference information for installing and configuring the ECDR-GC814 board.

- CY7C960 and CY7C961 User's guide, Cypress Semiconductor Corp.
- AD6645 Data Specification, Analog Devices Corp.
- GC4016 Data Specification, Graychip Corp.
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- ANSI/VITA 1-1994 (VME64 Specification)
- ANSI/VITA 1.1-1997 (VME64 Extensions Specification)
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- The VMEBus Handbook, VMEbus International Trade Association (VITA)
- ECDR-GC814 Programmers Manual, Echotek Corp.
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Document Conventions

The following icons are used in this manual to emphasize setup or system information.

Icon	Use
	Alerts you to important details regarding the setup or maintenance of your system.
	Alerts you to potential damage to the board during system setup and installation.

Technical Support

If you need additional technical information or assistance in retrieving product documentation, contact Echotek Corporation.

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Chapter 1 Introduction

This chapter provides a general overview of the ECDR-GC814 board, lists the available product models, and describes operating modes and product applications.

ECDR-GC814

Echotek Corporation's ECDR-GC814 is an analog-to-digital (A/D) converter and digital drop receiver board. The ECDR-GC814 provides eight receiver channels of 14-bit, 80 MHz analog-to-digital conversion and digital processing suitable for wideband and narrowband down conversion and filtering in a single 6U VME slot. Refer to Figure 1-1 for the ECDR-GC814 block diagram.

For applications requiring raw A/D data *only*, the ECDR-GC814 A/D is available. However, since the receiver section of each channel can be bypassed to output raw A/D, the standard ECDR-GC814 board can also be used for applications requiring raw A/D data. All configuration options are available in two-, four-, or eight-channel models.

Features

- Analog Devices AD6645 converter
- Eight input channels, 14-bit, 80 MHz analog-to-digital conversion
- Configuration options available in two, four, or eight input channel models
- SFDR in excess of 90 dBFS
- FIFO buffer is 16K x 32 bits; factory configurable up to 128K x 32 bits
- VME64X interfaces

- Two operating modes: Gate Mode and Counted Burst
- Fixed full-scale of 1.1 Vpp (+5 dBm)
- Graychip GC4016 digital receiver chip
- Three output data formats supported: 16-Bit Complex, 20-Bit Complex, and 16-Bit Real
- Input channels can support four independent receiver channels in narrowband mode with each having a decimation from 32 up to 16384
- Input channels can support a decimation from 8 up to 4096 when four narrowband receiver channels are combined
- Each input channel contains four NCO (Numerically Controlled Oscillator) Mixers with 0.02 Hz Tuning Resolution
- Each receiver channel also contains a 5-Stage CIC Filter, one Programmable 21 Tap FIR Filter, one Programmable 63 Tap FIR Filter, one 256 Tap Resampler FIR Filter

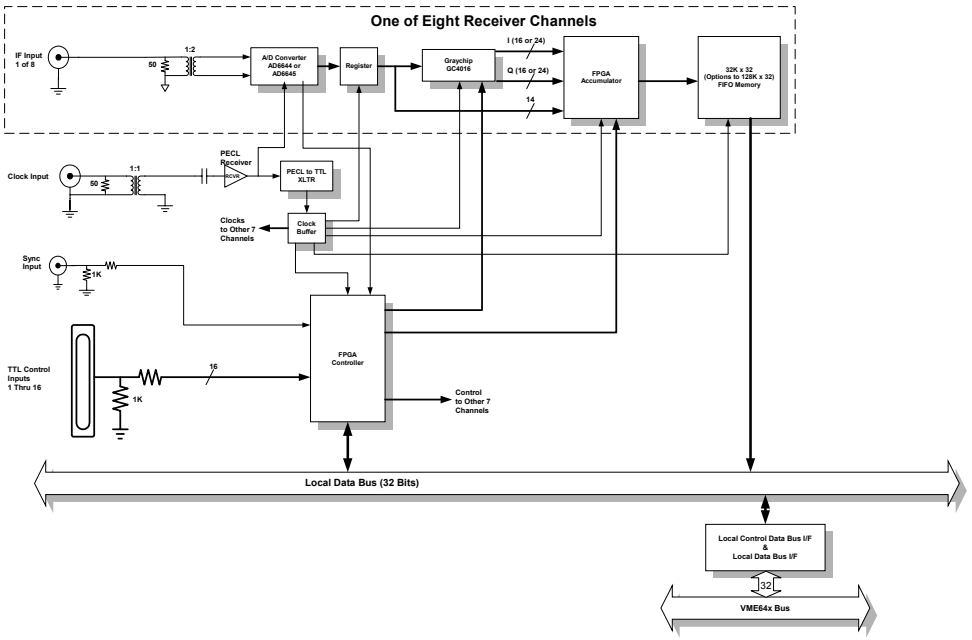

Figure 1-1 ECDR-GC814 Block Diagram

ECDR-GC814 Models

Table 1-1 includes the ECDR-GC814 models that are currently available from Echotek Corporation. See Chapter 2 Product Overview for more information on each model. For additional configurations, please contact Echotek Corporation.

Table 1-1 ECDR-GC814 Models

Model	Features
ECDR-GC814/8	Eight channels with one GC4016 receiver chip per channel
ECDR-GC814/4	Four channels with one GC4016 receiver chip per channel
ECDR-GC814/2	Two channels with one GC4016 receiver chip per channel
ECDR-GC814/8-A/D	Eight A/D channels, no receiver chip
ECDR-GC814/4-A/D	Four A/D channels, no receiver chip
ECDR-GC814/2-A/D	Two A/D channels, no receiver chip

Data Inputs

The ECDR-GC814 board is designed to receive the following inputs through the front panel SMA connectors:

- Eight analog signals
- A/D clock
- Sync signal
- Up to a 16-bit wide digital word

The eight analog signals that can be input to the ECDR-GC814 board through the front panel SMA connectors are converted using Analog Devices AD6645, 14-bit, 80 MHz A/D converters. The A/D converters are high quality and exhibit spur free dynamic ranges (SFDR) in excess of 90 dBFS (decibels full scale. In addition, the converters support direct digitization for Intermediate Frequencies (IF) up to 100 MHz.

The A/D clock, sync signal, and up to a 16-bit digital word also can be input through the front panel SMA connector. The clock signal (sine wave into 50 ohms) is buffered and distributed to all eight channels so that all channels are sampled simultaneously.

Receiver

The GC4016 receivers can be operated at 80 MHz clock rate. The decimation range of the receiver channels depends on the usage within one GC4016: one GC4016 may be operated as four independent channels, two independent channels, or one channel. For more information on bandwidths, decimation ranges, and FIFO sizes, see "Combining Receiver Channels" in *Chapter 2 Product Overview*.

FIFO Buffer

The FIFO buffer for each channel receives data that is output from the sample accumulator. The FIFO buffer is 16K x 32 bits (by default) and can be configured at the factory as large as 128K x 32 bits.

Data Output

Depending on the mode selected, the data output from the ECDR-GC814 can be either raw A/D data or complex receiver data.

Operating Modes

The ECDR-GC814 supports both continuous waveform (CW) and pulsed system applications. The board can be controlled in either of two basic operating modes:

Gate Mode - Data acquisition occurs when the gate signal is active. The gate signal can be provided through external front panel input or by a *write* software function.

Counted Burst - A preprogrammed number of samples is acquired and processed with each occurrence of an external trigger pulse. This trigger pulse also has a software bit counterpart associated with it.

Set-Up and Control

You can access all set-up and control registers through the VME interface. Refer to Chapter 4 Installation and Setup for more information.

Board Maintenance

The ECDR-GC814's "Programmable Logic," in the form of Electrically Programmable Logic Devices (EPLD)s and Field Programmable Gate Arrays (FPGA)s, provides the flexibility to make design modifications required for specific applications. The EPLDs and FPGAs are re-programmable on the board, enabling you to add new "features" as the need arises or to make "bug" fixes.

Note: For upgrading and retesting, please return the ECDR-GC814 to the vendor.

Product Applications

The ECDR-GC814 is designed to support a broad range of Digital Receiver applications including both pulsed and Continuous Wave (CW) applications, with or without coherence requirements.

Not only can raw A/D data be collected, but the onboard A/Ds also support applications that require processing analog base-band, in-phase/quadrature (I/Q) data. For these applications the GC4016 can be configured in two ways:

- To process the complex inputs as channel pairs (two output channels),
- To combine all four channels to provide a single wideband output channel.

Combining channels reduces the minimum required decimation, enabling the ECDR-GC814 to process information bandwidths of up to 2.5 MHz, 5 MHz, and 10 MHz for quad, dual, and single output channels. A 70 MHz rate is assumed.

Chapter 2 Product Overview

This chapter provides more detailed product features, including analog signal inputs, clocking, channel configurations, and A/D data.

Overview of the ECDR-GC814

The ECDR-GC814 board is designed to achieve the objectives of your particular application by providing two modes of data collection, four independently configurable channels, and the Graychip GC4016 Quad Narrowband Digital Receiver used in parallel output mode to maximize the output rate for wideband and narrowband applications. This receiver product has been optimized for continuous and coherent, pulsed real-time data collection of multiple synchronous channels, making it ideal for both digital radio and radar sensing applications.

The ECDR-GC814 board is designed to accept eight wideband analog inputs, digitize the inputs with 14-bit A/D converters, and then down convert and filter the digitized data for each input. The board then re-samples the data to adjust the output sample rate and stores the processed data to a sample FIFO memory for each receiver channel.

The ECDR-GC814 supports two modes of data collection: Continuous and Counted Burst. Both modes of data collection can use either an external input (Sync) or a software register bit to turn collection on and off. Synchronization logic synchronizes all channels on the ECDR-GC814 and any other ECDR-GC814s in the system when cabled properly.

The functional elements of the ECDR-GC814 are described in more detail in the following sections.

Board Configurations

- **Analog Signal Input**

The ECDR-GC814 receives analog signals through the front panel SMA connectors, which are transformer coupled and are 50 Ω impedance. The inputs have a full-scale input of 1.1 Vpp (+5 dBm). Data is then routed through a Mini-Circuits transformer (ADT4-6WT) with a 6 dB bandwidth of 2 MHz to 300 MHz (For other footprint compatible transformers that you can use, contact Echotek for details). The analog signals then are input to the AD6645, a 14-bit, 80 MHz A/D converter.

- **Clock Logic**

You must input the clock through the front panel SMA connector. The clock signal is buffered and distributed to all eight channels so that all channels are sampled simultaneously. Specific requirements for the clock are the following:

- -2dBm (0.5Vpp) to +4dBm (1Vpp)
- 80 MHz maximum rate A/D sample rate and 90 MHz maximum receiver clock
- Sine Wave preferred (see below)
- 50-Ohm input

The clock is received by a Positive Emitter Coupled Logic (PECL) receiver, which is AC-coupled to the input with a 50-Ohm termination. AC coupling of the input blocks the DC voltage, enabling AC peak-to-peak voltage to be received.

The clock amplitude range is -2dBm (0.5Vpp) to +4dBm (1Vpp), but smaller levels can provide a good clock. If the input is considerably larger than +4dBm (1Vpp), the receiver can be damaged permanently.

The external clock is buffered and provides 1:1 clocking to all the A/D converters. This same clock is also distributed to the GC4016 digital receivers. You can choose to clock the digital receivers at the same rate or twice the rate of the A/D converters. The clock rate selection is done in groups of four channels (channels 0-4 and/or 3-7).

If the A/D converters are operated at the same rate as the receivers, the maximum clock rate is 80 MHz. However, if you are operating any of the receivers at twice the clock rate of the A/D converters, the maximum input is 45 MHz.

We recommend that you operate the GC4016 digital receiver clock at the highest possible rate, since this permits the largest number of filter taps to be used for a given filter design. We also recommend that you operate the A/D at the highest possible clock rate since the receiver "processing gain" is achieved through the reduction of noise bandwidth via the filtering and associated data rate decimation process. Refer to the GC4016 data sheet for more information on filter configurations.

NOTE: For PLL Stabilization, bits 2 and 3 in the CSR (see Register Map) must be set based upon the clock frequency.

We recommend that you use a low phase noise sine wave as a source. However, if you use a square wave, select a 50 percent duty cycle with very low jitter. Any phase noise (jitter for a square wave) on the input directly translates as distortion in the A/D converter and is reflected in the digitized data.

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- **Trigger Logic**

Data acquisition can be initiated by either an external trigger or by a software initiated trigger.

  - **External Trigger**

    You must input the trigger through the front panel SMA connector. The trigger signal is buffered and distributed to all eight channels. Specific requirements for the trigger are specified in chapter 3. CSR bit 4 must be set to a 1 to enable external trigger.

  - **Software Trigger**

    To disable external trigger, CSR bit 4 must be set to a 0. Writing a 1 to CSR bit 9 is then the software equivalent to the external SYNC (trigger) pulse.

- **Header Word**

An input connector is provided to enable the insertion of a 16-bit wide digital header word into the data stream or for tagging data. This word is latched in on the rising edge of the sync signal and is available for you to read as needed.

- **DATA READ Modes**

The acquired data can be read from the FIFO'S by single cycle access or by using DMA. Throughput for DMA will be improved if the DMA_Look_Ahead mode is utilized. To use Single Cycle Mode, bit 14 of the CSR register must be set to a " 0 " prior to acquiring data. To use the "DMA_Look_Ahead" mode, bit 14 of the CSR register must be set to a "1" prior to issuing the "Local Start Address & Go" command.

Note: Refer to the Cypress Semiconductor Corporation's CY7C961 User's Guide for setting:

- Block Count
- Transfer Type
- Local Start Address

Note: D64 Block transfers can be run as 256-Byte Boundary or as 2K-Byte Boundary. To run the 2K-Byte boundary requires setting the switch (S3 position 4) to Interleave Disable and setting bit 1 of the CSR register to enabled.

Channel Configurations

The ECDR-GC814 board supports the following data collection modes, whether you are using a 2-, 4-, or 8-channel configuration.

- Acquire raw A/D data
- Acquire and process the data through the Graychip

Table 2-1 shows the configurations and the corresponding input channels available on the ECDR-GC814 board. For example, signals received by an ECDR-GC814 configured with two channels are input into channels 0 and 2. The registers for channels 0 and 2 handle the control for data collection.

The registers for channels 1 and 3 respond to VME access, but do not perform any control function. Channels 4 through 7 do not respond to VME access in a configuration of two channels.

Table 2-1 ECDR-GC814 Board Configuration and Input Channels

Board Configuration	Signal Input Channels
Two Channels	Channels 0 and 2
Four Channels	Channels 0, 2, 4, 6
Eight Channels	Channels 0 – 7

Signals received by an ECDR-GC814 configured with four channels are input into channels 0, 2, 4, and 6. The registers for channels 0, 2, 4, and 6 handle the control for data collection. The registers for channels 1, 3, 5, and 7 respond to VME access, but do not perform any control function

• Data Acquisition Modes

The ECDR-GC814 has been designed to support data acquisition for both CW and pulsed system applications. An SMA connector external sync input on the front panel supports two operating modes: Trigger mode, which collects data with each occurrence of an external trigger pulse; and Gate mode, which provides control of the data processing interval based on an external signal.

o Gate Mode

The ECDR-GC814 provides a Gate mode where you can input an external signal to control the data collection. In the Gate mode, data is collected as long as the Gate signal is active; however, data can be lost if you can not move the data out of the FIFO faster than it is being generated.

o Trigger Mode

The Trigger mode treats the external trigger input or the Software Sync Bit like a synchronizing "trigger." With the Free Run bit set to "0" the rising edge of the trigger initiates the collection of a software-programmed number of data samples. Note that the programmable counter is 17 bits wide (18 bits wide if using Fifo Ping Pong mode), permitting collection of up to 128K sample pairs, which is the maximum depth of the FIFOs. If the Free Run bit is set to "1," then data collection begins when the external trigger is received and continues until the Trigger Clear bit is written. Data can be lost if it cannot move out of the FIFO faster than it is being generated.

Note: Refer to Table 6-11 for control of Trigger or Gate Mode. Refer to Table 6-12 for control of Burst Counter (Data Window Size/DWS).

- **Delayed Trigger**

Delayed Trigger can be used in Trigger Mode only. The trigger signal (either S/W or external trigger) can be delayed to each pair of channels (0,1 & 2,3 & 4,5 & 6,7). To enable the delay requires setting the SYN_DLY_ENABLE bit to a 1. This is done by setting bit 28 of the channel CSR register. To set the time delay requires loading the SYNC_DELAY Counter for each pair of channels. Each pair of channels will start acquiring data based on the programmed delay. The counter is a 12 bit counter that is clocked at the A/D sample rate.

- **Trigger Counter**

The Trigger Counter can be used in Trigger Mode only. "TDONE" is an interrupt that is generated from the terminal count of the Trigger Counter. The Trigger Counter is loaded to the value of the desired # of triggers to acquire before

Trigger Done (TDONE) Interrupt is issued. This is a 17 bit counter and the max count is 1FFFFh.

• Data Selection

As shown in the block diagram figure 1-1, multiple paths are available for data collection. Data can be obtained from the receivers as either packed or unpacked. Data can be obtained from the A/D and handled as raw, thinned or samples truncated into 8 msb's (8 bit packing). The channel CSR register, bits 0 and 1 and DATA_SEL register bits 0 and 1 control the selection of data.

o Receiver Data

Refer to "Receiver Channels section" to obtain additional information on the GC4016 receiver. The Receiver –Skip mode is only available when collecting data through the receivers.

- Packed Mode
  Sixteen (16) bits of " I " data and 16 bits of " Q " data are packed into each 32bit word.
- Unpacked Mode
  Twenty-four (24) bits of " I " data and 24 bits of " Q " data are output in sequential 32 bit words.
- Receiver Skip Mode
  Inhibits the collection of valid Receiver Data samples based on the value loaded into RSKIP for each channel. Refer to Table 6-13.

o A/D Data

A channel can be configured to acquire raw A/D data with a sample rate up to 80 mega-samples per second (MSPS).

- Raw A/D data
  The raw samples are stored in the FIFO as a 32-bit word composed of two 16-bit samples. These samples are right justified with the two least significant bits (LSB)s always set to zero so that the data can be processed as 16-bit data.
- 16 Bit Data Thinning
  A/D data can be thinned by a factor of from 2 to 64 on a per channel basis. Loading the THIN_CNT register to the appropriate value controls thinning rate. Refer to Table 6-16.
- 8 Bit Data Packing
  A/D data can be truncated to the 8 MSB's and packed 4 samples to a 32 bit word.

- **FIFO Control**

FIFO memory for CH 0, 2, 4 and 6 can be extended into FIFO memory for CH 1, 3, 5 and 7 respectively, but at a sacrifice of data collection for Ch 1, 3, 5 and 7. This essentially doubles the FIFO size for CH 0, 2, 4 and 6. This is a ping-pong action where a counter is set to the number of words to be written into the first FIFO and upon termination of count, data is then written into the second FIFO. Total number of words written is based upon DWS. To initiate the PING_PONG control set bit 2 of the Data_Sel register (reference Table 6-14) and load the FIFO Word counter (reference Table 6-15).

- **Receiver Channels**

The ECDR-GC814 consists of eight independent channels, each having one GC4016 channel, data formatting logic, and one sample FIFO as shown in Figure 2-1. You can configure each channel independently, based on the requirements of your application.
Each GC4016 receiver channel includes a five-stage Cascaded Integrator Comb (CIC) filter, a programmable 21-tap Symmetrical FIR (Finite Impulse Response) filter, a programmable 63-tap Symmetrical FIR Filter, and a symmetrical 512-tap Resampler FIR filter. The 21-tap Symmetrical FIR filter can be operated as an 11-tap non-symmetrical FIR filter; the 63-tap symmetrical FIR filter can be operated as a 32-tap, non-symmetrical FIR filter.

Note: For more information about the Cascaded Integrator Comb filter, refer to "An Economical Class of Digital Filters for Decimation and Interpolation" by Eugene B. Hogenauer, IEEE Transactions on Acoustics, Speech, and Signal Processing, Volume ASSP-29, Number 2, April 1981. For more information on the Graychip GC4016 Digital Receiver, refer to the GC4016 Data Specification document.

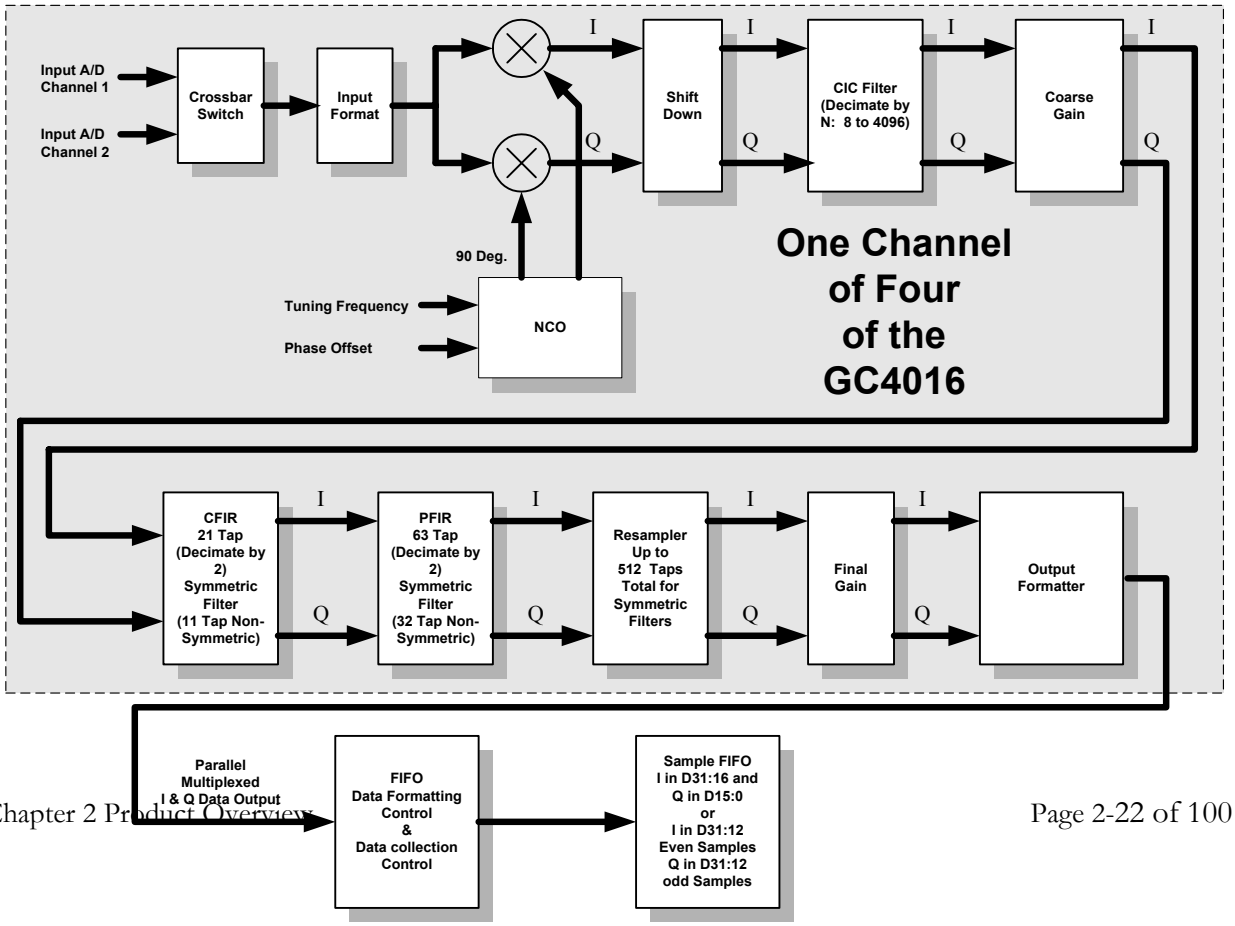

Figure 2-1 Functional Diagram of GC4016 Receiver Channel

Each receiver channel has a standard 32-bit wide sample FIFO memory bank for storage of the following input data: NOTE: All data is 2's complement.

- All 16-bit complex samples are 16 bits of In-Phase (I) and 16 bits of Quadrature (Q) data with I and Q packed into one 32-bit word (I in D31:16, and Q in D15:0).
- All 20-bit complex samples are 20 bits of In-Phase and 20 bits of Quadrature data with I and Q sequentially stored into two 32-bit words (first sample I in D31:12, and the second sample Q in D31:12). The unused LSB's are zeroes.
- All 16-bit real samples are 16 bits of real data with two sequential samples packed into one 32-bit word (1st sample in D31:16, 2nd sample in D15:0).

All critical parameters of the receiver channels can be updated synchronously with each other and with other ECDR-GC814 boards.

Combining Receiver Channels

You can configure the four receiver channels as four narrowband channels, two wideband channels, or one extra-wide band channel, depending on the requirements of your product application. Refer to Table 2-2 below for bandwidths, decimation ranges, and FIFO sizes for each configuration.

Table 2-2 Combining Receiver Channels

Receiver Channels	Maximum Bandwidth*	Minimum Bandwidth*	Decimation Range	FIFO Size
4 narrowband	2.5 MHz	2.441 kHz	32 to 32768	Channels 1 through 4
2 wideband	5 MHz	4.882 kHz	16 to 16384	Channels 1 and 2 only
1 extra-wide band	MHz	9.766 kHz	8 to 8192	Channel 1 only

* The maximum and minimum bandwidths are given for a clock rate of 80 MSPS (mega-samples per second).

Synchronization

The synchronization logic is designed to synchronize channels on one or more ECDR-GC814 boards in the system. Table 2-3 lists the four sources that can trigger a "sync" signal and the behavior of each source. As shown in the table, you can program the software-controlled register, the GC4016 internal control, or the GC4016 sync out register to provide a synchronization signal and synchronize multiple boards in the same system for both collection modes.

The Sync input pulse synchronizes the receiver channels at the start of data collection (Data Window) as would be done when the ECDR-GC814 is used in a pulsed, coherent system. In the Gate Continuous Collection Mode, the external Sync input can be used solely as a synchronization signal to synchronize all receiver channels, but it must be synchronous with the input clock, and meet setup and hold time requirements to function properly.

To use the board in a pulsed, coherent system, use the Sync input pulse at the start of the Data Window.

Table 2-3 Sources of Synchronization Signal

Sync Signal Sources	When occur?	Multiple ECDRs?	Both Collection Modes?
1. ECDR-GC814 register	Anytime	No	Yes
2. GC4016 internal control	Anytime	No	Yes
3. GC4016 sync out register	Anytime	No	Yes
4. External Gate/Trig input			
▪ Control Collection Only	No syncing from signal	No	Yes
▪ Sync + No Control Collection	Syncs when signal becomes active	Yes	Yes
▪ Sync + Control Collection	Syncs when signal becomes active	Yes	Yes

Chapter 3 Specifications

This chapter provides the following specifications for the ECDR-GC814 board:

- General Specifications
- Power Requirements
- Environmental Specifications

General Specifications

Physical Specifications	
Size	VME 6U
Interface	VME64X Only
Number of AD channels	2, 4, 8
Number of Receiver Channels	4 per A/D channel
A/D Converter Type	AD6645
VME Interface	Cypress CY7C961
Connector Specifications	
Input connector	Coax Type SMA
Header words	AMP 104066-1 (mating connector 111196-4)

External Input Interface Specifications

A/D Channel 1 Input	
Input Voltage Range	+5dBm Max
Input Type	Transformer Coupled
Input Impedance	50 Ohms
Input Frequency Range (3dB)	500 kHz to 600 MHz
Sync Input	
Input Voltage Range	0 to +4V
Threshold	2.4V, TTL Logic
Input Type	Single Ended
Input Impedance	1000 Ohms
High Time	2 Receiver Clocks minimum
Low Time	2 Receiver Clocks minimum
Setup Time	Set-up time for Sync is +5ns prior to rising clock edge. Use the "Leading midpoint of clock waveform" as reference to set-up time for Sync input.
Hold Time	Hold-time should be a minimum of 2 clock periods in duration and measured from leading edge of Sync
External Clock Input	
Input Voltage Range	-2 dBm to +4 dBm (0.5Vpp to 1Vpp)
Input Type	Single Ended, AC Coupled
Input Impedance	50 Ohm
Frequency Range	20 MHz to 80 MHz (A/D max) 20 MHz to 90MHz (Receiver max)

Power Requirements (typical)

Configuration	+5Vdc	+3.3Vdc	+12Vdc	-12Vdc	Power
ECDR-GC814/8	3.6 Amps	3.2 Amps	n/a	n/a	28.6 Watts
ECDR-GC814/4					
ECDR-GC814/2					
ECDR-GC814/8-AD					
ECDR-GC814/4-AD					
ECDR-GC814/2-AD					

Environmental Specifications

Parameter	Operating	Storage
Temperature	0- 55 ° C	-55 °C - + 100 °C
Relative Humidity	95% Non-Condensing	95% Non-Condensing
Cooling Requirement	A Linear Air Flow of > 2.5 Meters/sec is recommended.	N/A
Thermal Shock	5 °C/MIN	10 ° C/Min
Altitude	-1000 – 10000 Feet	-1000 – 50000 Feet
Vibration	10 to 100 HZ @ 2G	10 to 500 HZ @ 2G
MTBF	> 100,000 Hours	N/A
Mechanical Shock	20G for 6 MS (Half Sine) when mounted in a suitable racking system	

Chapter 4 Installation and Setup

This chapter provides board installation and setup information, including setting switches and connectors.

Unpacking the Product

Before unpacking the product, note the following guidelines:

- Check the shipping carton for damage. If the product's shipping carton is damaged upon arrival, request that the carrier's agent be present during unpacking and inspection of module(s).
- Make sure that the area designated for unpacking the product is a static electricity-controlled environment.
- Unpack the ECDR-GC814 board *only* on a grounded conductive pad using an anti-static wrist strap grounded to the pad**.**
- If moving the board is necessary, move it in an ESD protective container.

Note: The ECDR-GC814 board is shipped in an ESD protective container**.**

- Always avoid touching areas of integrated circuitry as static discharge can damage circuits.

After unpacking the product, check the contents of the container against the packing slip to verify that all items are present and undamaged**.**

ECDR-GC814 Board Switches

The switches provided on the ECDR-GC814 board are as follows:

- S1 - Enables you to bypass the VME Bus Grant signals; these signals are normally off.
- S2 - Sets the VME Bus request, which is used when the ECDR-GC814 is the bus master.
- S3 - Controls the VME Bus Interrupt Level, used by the ECDR-GC814 when interrupts are enabled.
- S3 Position 4 controls DMA Interleaving. The default setting for this switch is " **OFF**. " This sets the CY7C961 to have an interleave period at 256 byte boundaries. To operate at 2K byte boundaries, set Switch S3 Position 4 to " ON " and set the D64_2K_ENABLE bit to a 1 (see Table 6-3 bit1).

  Note:
  The time between bursts is known as the interleave period. The length of the interleave period is configurable in BTCR[3:0]. During the interleave period, slave cycles can be performed. Master cycles are allowed if the dual-path feature is enabled. For BLT transfers, the CY7C961 will cross VME address boundaries without releasing the VMEbus unless the Interleave function is programmed on. The CY7C961 can be programmed through the initialization bit stream to release and re-request the VMEbus at every 256-byte boundary as DMA transfer progresses. This behavior can be useful in providing VMEbus access to high-priority traffic

interleaved with the DMA transaction. The CY7C961 can be programmed through the initialization bit stream to release and re-request the VMEbus at every 2K-byte boundary to perform a faster DMA.

- S4 - Sets the base address of the ECDR-GC814 in the VME Bus A32 address space.

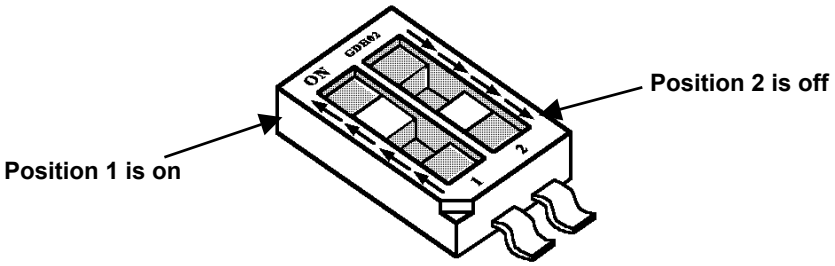

Figure 4-1 Setting Switches on the ECDR-GC814

As shown above, enable the **ON** position by pushing the slider towards the side of the switch where the word **ON** is printed. To enable the **OFF** position, push the slider away from the side of the switch where the word **ON** is printed.

Note: In the event that the word *ON* has been rubbed off, remember that the ON position is on the opposite side of the beveled corner.

Setting Switches

Set the S1 through S5 switches on the ECDR-GC814 board as shown in the following tables.

S1 - Bus Grant Daisy Chain 0 through 3 Bypass	Pos 4	Pos 3	Pos 2	Pos 1
Bus Grant 0 Bypass	off	off	off	off
Bus Grant 1 Bypass	off	off	on	off
Bus Grant 2 Bypass	off	on	off	off
Bus Grant 3 Bypass	on	off	off	off

S2 - Bus Request 0 through 3	Pos 2	Pos 1
Level 0 Selected	on	on
Level 1 Selected	on	off
Level 2 Selected	off	on
Level 3 Selected	off	off

S3 - Interrupt Level and VME DMA Interleave Enable (switch is read at power-up only)	Pos 4	Pos 3	Pos 2	Pos 1
No Interrupt	X	on	on	on
Interrupt Level 1 Select	X	on	on	off
Interrupt Level 2 Select	X	on	off	on
Interrupt Level 3 Select	X	on	off	off
Interrupt Level 4 Select	X	off	on	on
Interrupt Level 5 Select	X	off	on	off
Interrupt Level 6 Select	X	off	off	on
Interrupt Level 7 Select	X	off	off	off
VME DMA Interleave Enable	off	X	X	X
VME DMA Interleave Disable	on	X	X	X

S4 - Base Address		
Position	**Address Bit**	**Example Address Setting 0Dxxxxxx**
8	A31	On - (0)
7	A30	On - (0)
6	A29	On - (0)
5	A28	On - (0)
4	A27	Off - (1)
3	A26	Off - (1)
2	A25	On - (0)
1	A24	Off - (1)

Connectors

Input Connectors

Connector	Function 8 Channel Configuration	Function 4 Channel Configuration	Function 2 Channel Configuration
J1A	Channel 0 Input (SMA)	Channel 0 Input (SMA)	Channel 0 Input (SMA)
J1B	Channel 1 Input (SMA)	NA	NA
J1C	Channel 2 Input (SMA)	Channel 2 Input (SMA)	Channel 2 Input (SMA)
J1D	Channel 3 Input (SMA)	NA	NA
J1E	Channel 4 Input (SMA)	Channel 4 Input (SMA)	NA
J1F	Channel 5 Input (SMA)	NA	NA
J1G	Channel 6 Input (SMA)	Channel 6 Input (SMA)	NA
J1H	Channel 7 Input (SMA)	NA	NA
J2	External Clock Input (SMA)	External Clock Input (SMA)	External Clock Input (SMA)
J3	External Sync Input (SMA)	External Sync Input (SMA)	External Sync Input (SMA)
J4	Header Input	Header Input	Header Input

Header Input (J4) Pin Functions
Logic 1: 2 to 5.5 Vdc
Logic 0: -0.5 to 0.8 Vdc

Pin	Function
1	Ground
2	Ground
3	Header Bit 0
4	Header Bit 1
5	Header Bit 2
6	Header Bit 3
7	Header Bit 4
8	Header Bit 5
9	Header Bit 6
10	Header Bit 7
11	Header Bit 8
12	Header Bit 9
13	Header Bit 10
14	Header Bit 11
15	Header Bit 12
16	Header Bit 13
17	Header Bit 14
18	Header Bit 15
19	Ground
20	Ground

Chapter 5 Operating Guide

This chapter provides information for connecting inputs to signal sources, configuring the VME Bus and the GC4016s, and synchronizing operation and control.

Connecting to the IF Inputs

After installing the ECDR-GC814, connect the IF inputs to the signal source. Read these guidelines carefully before you begin.

- Check for proper signal level. The IF inputs can accept a signal of up to +/-0.56Vp Max (+5 dBm).

The input impedance is 50 Ohms. The signal source must be able to drive the impedance to the required signal level. A signal level greater than +/- 0.56Vp Max (+5 dBm) saturates the A/D and can damage the A/D converters. The maximum signal that will not damage the A/D converters is +/- 1.1 Vp; however, this signal will prevent the A/D converter from outputting valid data.

- If the signal level is unacceptable (greater than +5 dBm), use an in-line 50-ohm attenuator to drop the signal level to an acceptable level.
- Use a high quality cable with matched 50-Ohm characteristic impedance; make sure the source is shielded and has a good ground connection. Using high quality cable is important to prevent very small and undesired signals and noise from being "picked up" by the cable.
- Correctly ground the complete system. To prevent the introduction of noise to the A/D converters, ensure that no ground differences exist between the source and the ECDR-GC814.
- Use an SMA adapter to the required cable type or an SMA-type cable to connect the inputs.

Connecting to the Clock Input

After you have connected the IF inputs to the signal source, connect the clock signal source to the clock input. Read these guidelines carefully before you begin.

- Check the clock source for proper signal level. The signal level should be within an input range of -2 dBm to +4 dBm. The source must be able to drive the input impedance of 50 Ohms to the minimum input level. The minimum signal that can be received correctly is +/- 0.25Vp (-2 dBm).
- We recommend that you use a low phase noise sine wave as a source. However, if you use a square wave, select a 50 percent duty cycle with very low jitter.

Any phase noise (jitter for a square wave) on the input directly translates as distortion in the A/D converter and is reflected in the digitized data.

- Use an SMA adapter to the required cable type or an SMA-type cable to connect the clock inputs.

Connecting to the Gate/Trig Input

After connecting the clock signal source to the clock input, connect the signal source to the Gate/Trig input. Read these guidelines carefully before you begin.

- Use a TTL level input signal. The input impedance is 1K Ohms, which for most sources is high impedance. If you are connecting a 50-Ohm source, halve the output voltage you

would normally use. For example, if 0V to 3V is the required signal level, set the signal generator output to 0V to 1.5V.

- Use a square wave input with fast rise and fall times of about 5nSec. This input operates optimally when it is synchronized with the input clock and meets the setup and hold times as specified in Chapter 3 Specifications.

For counted burst applications, this input is a pulse, and must be at least one input clock wide. For continuous gate applications, this input may be any size above one of the receiver output clocks (the decimated clock rate that the receiver channels will output). For example if the input clock is 80 MHz, and the total receiver decimation is 16, then a minimum gate width of 200nSec should be used (the output clock rate is 80 MHz/16 = 5 MHz; the clock period = 200nSec).

When Gate/Trig input is not synchronous with the input clock, jitter is introduced on the Gate/Trig signal dependent upon the input clock period (+/- 1 clock of jitter). The jitter only pertains to when the collection is started and not to the sample clock.

Data Collection Modes

This section provides instructions for configuring and initializing the ECDR-GC814 for the three data collection modes: Gate Continuous, Free Run, and Counted Burst. Before you perform these operations, however, you should decide on the appropriate collection mode for your product application. Table 5-1 provides a list of options you should consider, including the number of channels to be used, type of data, signal source, and synchronization method. Table 5-2 lists a general order in which registers should be written to perform data acquisition.

Table 5-1 Selecting a Data Collection Mode

Configuration Items	Options
Collection Mode	Gate Continuous Free Run Counted Burst
Channels	1 4 2 8
Type of Collection Data	Raw A/D Data Receiver Data Complex Data – Packed (16 – bit) Complex Data – Unpacked (20- bit) Test Counter Data
Gate/Trigger Source	External Sync Input Register Control

Data Format

All A/D and Receiver data is 2's complement. The following three modes are available:

- Raw A/D Data
- Receiver Data Packed
- Receiver Data Unpacked

Raw A/D Data

Bit 31-16	Bit 15-0
Sample 0	Sample 1
Sample 2	Sample 3

- **Raw A/D Data Truncated and Packed (8 Bit Packing)**

Bit 31-24	Bit 23-16	Bit 15-8	Bit 7-0
Sample 0	Sample 1	Sample 2	Sample 3

- **Raw A/D Data with 16 Bit thinning**
  - Thin X2

Bit 31-16	Bit 15-0
Sample 0	Sample 2
Sample 4	Sample 6

- **Raw A/D Data with 16 bit thinning**
  - Thin X4

Bit 31-16	Bit 15-0
Sample 0	Sample 4
Sample 8	Sample 12

- **Raw A/D Data with 16 bit thinning**
  - Thin X8

Bit 31-16	Bit 15-0
Sample 0	Sample 8
Sample 16	Sample 24

Receiver Data Packed

This mode is not applicable when the ECDR-GC814 is used as an A/D board.

Bit 31-16	Bit 15-0
Sample 0 – I	Sample 0 – Q
Sample 1 – I	Sample 1 – Q

Receiver Data Unpacked

This mode is not applicable when the ECDR-GC814 is used as an A/D board.

Bit 31-12	Bit 11-0
Sample 0 – I	0
Sample 0 – Q	0

Header Format

The following two-word header can be read as status.

Note: Consult Echotek Corporation, if other headers are required.

<table>
<tr><th colspan="32">Header Format</th></tr>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">Channel Out of Range
(Out of Range = 1)</td><td colspan="24">Packet Count (Incremented on each trigger)</td></tr>
<tr><td colspan="8">FIFO Empty
Ch 7- Ch 0
(Empty = 1)</td><td colspan="8">FIFO Full Ch 7 – Ch 0
(Full = 1)</td><td colspan="16">Header Word From External Connector Bit 15-0</td></tr>
</table>

Configuring the VME bus

To configure the board for VME access, you must set Switches S1 - S4 to work with your system. See "ECDR-GC814 Board Switches" and "Setting Switches" in *Chapter 4 Installation and Setup* for details.

Configuring the GC4016

The following sequence enables you to set the GC4016 to a known state without causing random outputs and also synchronizes the four channels.

Table 5-2 Configuring the GC4016

Order	Operation	Result
1	Write 0x00 to GENERAL_SYNC.	Configures the GC4016 Local Bus.
2	Write 0xF8 to GLOBAL_RESET.	Holds the GC4016 in Reset.
3	Configure the GC4016; select the NCO Sync in the GC4016 register to be SIA input.	Configures the GC4016.
4	Write 0x03 to SCMD, SYNC Commands Register.	Holds the GC4016 in Sync.
5	Write 0x08 to GLOBAL_RESET.	Releases the GC4016 Resets.
6	Write 0x0 to SCMD, SYNC Commands Register.	Turns on the GC4016.

Setting Registers on the GC4016

Table 5-3 provides a list of values that must be used to correctly set registers for the ECDR-GC814.

Table 5-3 Setting Registers on the GC4016

GC4016 Register	Register Value (Binary)	Description
Global Reset	XXXX 1XXX	Edge Write must be ENABLED.
General Syncs	00XX XXXX	LVDS must be DISABLED. 4-Bit Address Mode must be DISABLED.
Tristate Controls	1111 1111 (FFh)	All Control Signal Outputs must be ENABLED.
Output Format	XXX0 1001	RDY Width must be ZERO. Tags must be ENABLED. SFS must be NON-INVERTED. RDY Must be NON-INVERTED. SCK must be INVERTED.
Output Mode	X11X 1100	Output Mode must be PARALLEL. Master must be ENABLED. Parallel Mode must be ENABLED. Nibble Mode must be DISABLED. LINK Mode must be DISABLED.
Output Frame Control	11XX XXXX	SFS Mode must be 3: SFS = Data VALID, RDY = Frame Sync
Output Word Size	XX10 1XXX	Bits Per Word must be 24 (Program value = 5).
Output Clock Control	XX00 0001	NSERIAL must be 0. SCK Divide must be 2 (Program value = 1).
Output Tag A	0001 0000 (10h)	I Tag must be 0; Q Tag must be 1
Output Tag B	0011 0010 (32h)	I Tag must be 0; Q Tag must be 3.
Output Tag C	0101 0100 (54h)	I Tag must be 4; Q Tag must be 5.
Output Tag D	0111 0110 (76h)	I Tag must be 6; Q Tag must be 7.

Synchronizing the Receivers

You must program the GC4016 sync source for each function inside the GC4016, but it is not necessary that these functions be synchronized alike. For example, the NCO Sync can be set for SIA input from the ECDR-GC814 logic, and the Decimation Sync can be set for ONE_SHOT.

Table 5-4 lists all the options available for synchronizing the receivers. Table 5-5 lists the functions of the GC4016 that can be synchronized. Each entry in the table shows how both the ECDR-GC814 and the GC4016 Sync sources must be programmed for the synchronization type.

Note: Only receiver functions on the GC4016 can be synchronized. There are no functions outside the GC4016 that can be synchronized.

Table 5-4 Options for Synchronizing Receivers

ECDR-GC814 Sync Source	GC4016 Sync Source	Notes
N/A	OFF (never active)	GC4016 never allows syncing of functions.
Sync Command Latched Sync Bit To Sync A	SIA (same as Sync A on the ECDR-GC814)	Holds the function(s) in Sync until the bit is cleared to a zero.
Sync Command Pulsed Sync Bit To Sync A	SIA (same as Sync A on the ECDR-GC814)	Pulses the Sync to the function(s) of the GC4016 one time.
Auto-Sync at Start of Data Window To Sync A	SIA (same as Sync A on the ECDR-GC814)	Pulses the Sync to the function(s) of the GC4016 one time at the beginning of a Data Window.
Sync A External Sync Input To Sync A	SIA (same as Sync A on the ECDR-GC814)	Pulses the Sync to the function(s) of the GC4016 one time whenever the External Gate/Trig input goes active.
GC4016 Sync Output To Sync A	SIA (same as Sync A on the ECDR-GC814)	Routes the GC4016 Sync Output signal to the SIA Input. Is dependent on the GC4016 programming of the Output Sync bit field of the General Sync Register.
Sync Command Latched Sync Bit To Sync B	SIB (same as Sync B on the ECDR-GC814)	Holds the function(s) in Sync until the bit is cleared to a zero.

Table 5-4 Options for Synchronizing Receivers (continued)

ECDR-GC814 Sync Source	GC4016 Sync Source	Notes
Sync Command Pulsed Sync Bit To Sync B	SIB (same as Sync B on the ECDR-GC814)	Pulses the Sync to the function(s) of the GC4016 one time.
Sync A External Sync Input To Sync B	SIB (same as Sync B on the ECDR-GC814)	Pulses the Sync to the function(s) of the GC4016 one time whenever the External Gate/Trig input goes active.
GC4016 Sync Output To Sync B	SIB (same as Sync B on the ECDR-GC814)	Routes the GC4016 Sync Output signal to the SIA Input. Is dependent upon the GC4016 programming of the Output Sync bit field of the General Sync Register.
N/A	ONE_SHOT	Pulses the Sync to the function(s) of the GC4016 one time when the ONE_SHOT command is written in the GC4016 Count Sync Register.
N/A	TC	The GC4016 internal Counter pulses the Sync to the function(s) whenever the counter reaches Terminal Count (TC). The GC4016 Counter must be programmed with the desired counter value. Refer to the GC4016 Data Sheet for the counter definition.
N/A	ON (always active)	GC4016 always syncs functions or holds function in sync depending on the function.

Table 5-5 GC4016 Functions for Synchronization

GC4016 Functions	Notes
DIAG_SYNC	Synchronizes the Checksum generator. This control is in the General Sync register of the GC4016.
COUNTER_SYNC	Synchronizes the Sync Counter. This control is in the Count Sync register of the GC4016.
FREQ_SYNC	The NCO Down Convert Frequency takes effect on this sync. This control is in the Frequency Sync Register of the GC4016 for each channel.
NCO_SYNC	The NCO is set to the current Phase register setting on this sync. This control is in the NCO Sync register of the GC4016. If the NCO is held in sync, then no data will be processed for each channel.
DITHER_SYNC	The NCO Dither Generator is reset to Zero on this Sync. This control is in the NCO Sync Register of the GC4016 for each channel.
ZPAD_SYNC	The Zero Pad Function is synchronized on this sync. This control is in the Zero Pad Mode Control Register of the GC4016 for each channel.
DEC_SYNC	The filtering (controlled by the Decimation Control Counter) is synchronized by this sync. This control is in the Dec and Flush Sync Register of the GC4016 for each channel.
FLUSH_SYNC	Flushes the channel. The channel should normally be flushed at initialization. You can flush the channel whenever new settings take effect to purge the data path. This control is in the Dec and Flush Sync register of the GC4016 for each channel.
GAIN_SYNC	The new Fine Gain takes effect on this Sync. This control is in the Decimation Ratio Byte 1 register of the GC4016 for each channel.
PEAK_SYNC	Synchronizes the Peak Counter Logic. This will update the read output register with the current counter value, and clear the counter. This control is in the Peak Control register of the GC4016 for each channel.
OUT_BLK_SYNC	Synchronizes the Output Logic of the GC4016. This control is in the Output Format register.

Chapter 6 Register Maps

This chapter provides memory maps and registers for the ECDR-GC814 board.

ECDR-GC814 Memory Map

This section includes the following register space tables:

- Baseboard Register Space
- DMA Controller Register
- Channel Register Space

Table 6-1 ECDR-GC814 Memory Map

Address Range Offset from Base Address	Description
00 0000h to 00 7FFCh	ECDR-GC814 Baseboard Register Space
00 8000h to 00 FFFCh	VME 961 DMA Controller Register
01 0000h to 01 FFFCh	CH[1..0] Channel Register Space
02 0000h to 02 FFFCh	CH[3..2] Channel Register Space
03 0000h to 03 FFFCh	CH[5..4] Channel Register Space
04 0000h to 04 FFFCh	CH[7..6] Channel Register Space
05 0000h to 07 FFFCh	Not Used
80 xxxxh	Channel 0 Data
90 xxxxh	Channel 1 Data
A0 xxxxh	Channel 2 Data
B0 xxxxh	Channel 3 Data
C0 xxxxh	Channel 4 Data
D0 xxxxh	Channel 5 Data
E0 xxxxh	Channel 6 Data
F0 xxxxh	Channel 7 Data

ECDR-GC814 Baseboard Register Space

This section includes a table for each Baseboard Register space.

Table 6-2 ECDR-GC814 Baseboard Register Space

Address Offset	Abbreviation	Register Name	Attribute
0 0000h	CSR	Command/Status Register	Read/Write
0 0004h	FLAGS	FIFO Flags	Read Only
0 0008h	INTVEC	Interrupt Vector	Read/Write
0 000Ch	INTMASK	Interrupt Mask	Read/Write
0 0010h	INTSTAT	Interrupt Status	Read Only
0 0014h	HEAD0	Header Word 0 Status	Read Only
0 0018h	HEAD1	Header Word 1 Status	Read Only
0 001Ch	TCNT	Trigger Counter	Read/Write
0 0020h		Not used	
0 0024h	TEST1	DMA Address Counter (Terminal count value)	Read Only For DMA Testing
0 0028h	TEST2	DMA Block Size	Read Only For DMA Testing
0 002ch	TEST3	DMA Block Size Terminal Count	Read Only For DMA Testing

Table 6-3 Command Status Register

Abbreviation	Width	Address Offset	Mask	Attribute
CSR		0 0000h		R/W

Least Significant Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																VME Only Bit 0: VME or RACEWAY can move data. 1: RACEWAY disabled, VME data moves only.
																D64_2K_Enable Bit This allows the VME Bus on card DMA Controller to perform D64 Block transfers and re-broadcast the address every 2K-Byte boundary only, otherwise it is every 256-Byte Boundary. Switch S3, Position 4 must be enabled . 0: Disabled (default) 1: Enabled.
																Frequency Select Bits Allow 15mS for the PLL to stabilize as changing these bits. 0h: LOW (12 MHz to 26 MHz) 1h: MID (24 MHz to 52 MHz) 2h: MID (24 MHz to 52 MHz) 3h: HIGH (48 MHz to 100 MHz)
																External Enable Bit 0: Idle 1: Opens path to accept the External SYNC pulse.
																Skew Control (Not Available) 0h: -4tu 1h: -3tu 2h: -2tu 3h: -1tu 4h: No Skew 5h: +1tu 6h: +2tu 7h: +3tu 8h: +4tu 9h – Fh: No Skew
																Software SYNC Bit (write only) Writing a 1h is the software equivalent to the SYNC pulse.
																Software Global GC4016 Sync Bit (write only) Writing a 1h will issue a sync signal that can be driven out to all the GC4016 if selected in the respective CSR_Cx registers.

Table 6-3 Command Status Register (continued)

Abbreviation	Width	Address Offset	Mask	Attribute
CSR		0 0000h		R/W

Least Significant Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Packet Count Clear (write only) Writing a 1h clears the packet counter used in the header.
																Local Bus Reset Bit (write only) Writing a 1h resets local bus.
																Not Used
																DMA Enable Bit 0= Single Cycle of FIFO Data 1= DMA of FIFO Data
																Not Used

Most Significant Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used
																Not Used
																PLL A Locked (read only) 0: PLL A is not locked 1: PLL A is locked to the input clock
																PLL B Locked (read only) 0: PLL B is not locked 1: PLL B is locked to the input clock
																Not Used

Table 6-4 FIFO Flags Register

Abbreviation	Width	Address Offset	Mask	Attribute
FLAGS		0 0004h		Read Only

Least Significant Word																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Channel 0 FIFO status 000 = FIFO empty 001 = Some data. 011 = FIFO => programmable almost empty (PAE) 111 = FIFO full
																Channel 1 FIFO Status 000 = FIFO empty 001 = Some data. 011 = FIFO => programmable almost empty (PAE) 111 = FIFO full
																Channel 2 FIFO Status 000 = FIFO empty 001 = Some data. 011 = FIFO => programmable almost empty (PAE) 111 = FIFO full.
																Channel 3 FIFO Status 000 = FIFO empty 001 = Some data. 011 = FIFO => programmable almost empty (PAE) **111 = FIFO FULL**

Table 6-4 FIFO Flags Register (continued)

Abbreviation	Width	Address Offset	Mask	Attribute
FLAGS		0 0004h		Read Only

Most Significant Word																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Channel 4 FIFO Status 000 = FIFO empty 001 = Some data. 011 = FIFO => programmable almost empty (PAE) 111 = FIFO full.
																Channel 5 FIFO Status 000 = FIFO empty 001 = Some data. 011 = FIFO => programmable almost empty (PAE) 111 = FIFO full.
																Channel 6 FIFO Status 000 = FIFO empty 001 = Some data. 011 = FIFO => programmable almost empty (PAE) 111 = FIFO full.
																Channel 7 FIFO Status 000 = FIFO empty 001 = Some data. 011 = FIFO => programmable almost empty (PAE) 111 = FIFO full.

Table 6-5 Interrupt Vector Register

Abbreviation	Width	Address Offset	Mask	Attribute
INTVEC		0 0008h		Read/Write

Least Significant Word																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**Description**
																Interrupt Vector 8-bit Interrupt vector driven on the bus when the ECDR-GC814 interrupt is acknowledged by the VME interface
																Not Used

Most Significant Word																
31	30	29	28	27	26	**25**	24	23	22	21	20	19	18	17	**16**	**Description**
																Not Used

Table 6-6 Interrupt Mask Register

Abbreviation	Width	Address Offset	Mask	Attribute
INTMASK		0 000Ch		Read/Write

Least Significant Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Channel 0 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled
																Channel 1 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled
																Channel 2 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled
																Channel 3 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled
																Channel 4 Data Available in the FIFO. Sets if the counted burst **is** complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled
																Channel 5 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled
																Channel 6 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled
																Channel 7 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled
																Not Used
																Not Used
																Not Used
																TDONE. Interrupt for trigger counter. 0h = Interrupt Disabled; 1h = Interrupt Enabled
																Not Used

Table 6-6 Interrupt Mask Register (continued)

Abbreviation	Width	Address Offset	Mask	Attribute
INTMASK		0 000Ch		Read/Write

Most Significant Word																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

Table 6-7 Interrupt Status Register

Abbreviation	Width	Address Offset	Mask	Attribute
INTSTAT		0 0010h		Read/Write

Least Significant Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Channel 0 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Channel 1 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Channel 2 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Channel 3 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Channel 4 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Channel 5 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Channel 6 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Channel 7 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Not Used
																Not Used
																Not Used
																TDONE. Occurs when number of triggers generated equals value loaded into TRIG COUNTER. 0h = No Interrupt; 1h = Interrupt Occurred
																Not Used

Most Significant Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

Table 6-8 Header Word 0 Status Register

Abbreviation	Width	Address Offset	Mask	Attribute
HEAD0		0 0014h		Read Only

Least Significant Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Packet Counter (Lower 16 Bits) These are the least significant bits to a 24-bit counter that counts the number of packets being collected at the A/D clock rate.

Most Significant Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Packet Counter (Upper 8 Bits) These are the most significant bits to a 24-bit counter that counts the number of packets being collected at the A/D clock rate.
																Channel 0 A/D Over Range Bit 0h = Not Over Range 1h = Over Range
																Channel 1 A/D Over Range Bit 0h = Not Over Range 1h = Over Range
																Channel 2 A/D Over Range Bit 0h = Not Over Range 1h = Over Range
																Channel 3 A/D Over Range Bit 0h = Not Over Range 1h = Over Range
																Channel 4 A/D Over Range Bit 0h = Not Over Range 1h = Over Range
																Channel 5 A/D Over Range Bit 0h = Not Over Range 1h = Over Range
																Channel 6 A/D Over Range Bit 0h = Not Over Range 1h = Over Range
																Channel 7 A/D Over Range Bit 0h = Not Over Range 1h = Over Range

Table 6-9 Header Word 1 Status Register

Abbreviation	Width	Address Offset	Mask	Attribute
HEAD1		0 0018h		Read Only

Least Significant Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																External Header Bits 16 header bits received through the J4 connector from an external source.

Most Significant Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Channel 0 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 1 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 2 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 3 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 4 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 5 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 6 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 7 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 0 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag
																Channel 1 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag
																Channel 2 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag
																Channel 3 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag
																Channel 4 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag
																Channel 5 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty **Flag**

Table 6-9 Header Word 1 Status Register (continued)

Abbreviation	Width	Address Offset	Mask	Attribute
HEAD1		0 0018h		Read Only

Least Significant Word																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Channel 6 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag
																Channel 7 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag

Table 6-10 Trigger Count Register

Abbreviation	Width	Address Offset	Mask	Attribute
TCNT		0 001Ch		Read/Write

Least Significant Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Trigger Count Value This is the counter that is loaded to the value of the desired # of triggers to acquire before Trigger Done (TDONE) Interrupt is issued. This is a 17 bit counter and the max count is 1FFFFh. See Chapter 2 "Trigger Counter" for more details.

Most Significant Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																MSB of Trigger Count Value
																Not Used

Table 6-11 DMA Address Counter (Terminal Address Counter)

Abbreviation	Width	Address Offset	Mask	Attribute
TEST 1		0 0024h		Read

Least Significant Word	
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	**Description**
	DMA Address Counter **This address can only be read after the " Local Start Address & Go instruction has been issued. Reading this address will give the terminal value of the address counter. The terminal count will equal the start address + block size.**

Most Significant Word	
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	**Description**
	Upper 16 bits of address counter

Table 6-12 DMA Block Size

Abbreviation	Width	Address Offset	Mask	Attribute
TEST 2		0 0028h		Read

Least Significant Word	
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	**Description**
	DMA Block Size **This address can be read before/after the " Local Start Address & Go instruction has been issued. Reading this address will give block size value and transfer type of the DMA.**

Most Significant Word	
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	Description
	MSB's of DMA Block Size
	DMA Transfer Type 0 = D32 1 = D64
	Not Used

Table 6-13 DMA Block Terminal Count

Abbreviation	Width	Address Offset	Mask	Attribute
TEST 3		0 002Ch		Read

Least Significant Word	
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	Description
	DMA Block Terminal Count **This address can only be read after the " Local Start Address & Go instruction has been issued. Reading this address will give the terminal value of the " DMA Block Size " counter. The counter is a down counter, so therefore the terminal count will equal " 0 ".**

Most Significant Word	
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	Description

ECDR-GC814 Channel Register Space

Address Offset	Abbreviation	Register Name	Attribute
01 0000h	CSR_C0	Command/Status Register Channel 0	Read/Write
01 0004h	DWS_C0	Data Window Size Channel 0	Read/Write
01 0008h	RSKIP_C0	Receiver Data Skip Channel 0	Read/Write
01 000Ch	DATA_SEL0	DATA_SEL Channel 0	Read/Write
01 0010h	CSR_C1	Command/Status Register Channel 1	Read/Write
01 0014h	DWS_C1	Data Window Size Channel 1	Read/Write
01 0018h	RSKIP_C1	Receiver Data Skip Channel 1	Read/Write
01 001Ch	DATA_SEL1	DATA_SEL Channel 1	Read/Write
01 0020h	FIFOCNT	FIFO WORD COUNTER	Read/Write
01 0024h	THIN_CNT0	Thin Channel 0 Word Counter	Read/Write
01 0028h	THIN_CNT1	Thin Channel 1 Word Counter	Read/Write
01 002Ch	SYN_DLY	Sync Delay CH 0 & CH 1	Read/Write
01 0030h – 01 0FFC		Not Used	
01 1000h – 01 17FCh	GC0	Receiver Register Space Channel 0*	Read/Write
01 1800h – 01 1FFCh	GC1	Receiver Register Space Channel 1*	Read/Write
01 2000h – 01 FFFCh		Not Used	Read/Write
02 0000h	CSR_C2	Command/Status Register Channel 2	Read/Write
02 0004h	DWS_C2	Data Window Size Channel 2	Read/Write
02 0008h	RSKIP_C2	Receiver Data Skip Channel 2	Read/Write
02 000Ch	DATA_SEL2	Data Select Channel 2	Read/Write
02 0010h	CSR_C3	Command/Status Register Channel 3	Read/Write
02 0014h	DWS_C3	Data Window Size Channel 3	Read/Write
02 0018h	RSKIP_C3	Receiver Data Skip Channel 3	Read/Write
02 001Ch	DATA_SEL3	Data Select Channel 3	Read/Write
02 0020h	FIFOCNT	FIFO Word Counter	Read/Write
02 0024h	THIN_CNT2	Thin Channel 2 Word Counter	Read/Write
02 0028h	THIN_CNT3	Thin Channel 3 Word Counter	Read/Write
02 002Ch	SYN_DLY	Sync Delay CH 2 & CH 3	Read/Write
02 0030h – 02 0FFCh		Not Used	Read/Write
02 1000h – 02 17FCh	GC2	Receiver Register Space Channel 2*	Read/Write
02 1800h – 02 1FFCh	GC3	Receiver Register Space Channel 3*	Read/Write
02 2000h – 02 FFFCh		Not Used	Read/Write

ECDR-GC814 Channel Register Space (Continued)

Address Offset	Abbreviation	Register Name	Attribute
03 0000h	CSR_C4	Command/Status Register Channel 4	Read/Write
03 0004h	DWS_C4	Data Window Size Channel 4	Read/Write
03 0008h	RSKIP_C4	Receiver Data Skip Channel 4	Read/Write
03 000Ch	DATA_SEL4	Data Select Channel 4	Read/Write
03 0010h	CSR_C5	Command/Status Register Channel 5	Read/Write
03 0014h	DWS_C5	Data Window Size Channel 5	Read/Write
03 0018h	RSKIP_C5	Receiver Data Skip Channel 5	Read/Write
03 001Ch	DATA_SEL5	Data Select Channel 5	Read/Write
03 0020h	FIFOCNT	FIFO Word Counter	Read/Write
03 0024h	THIN_CNT4	Thin Channel 4 Word Counter	Read/Write
03 0028h	THIN_CNT5	Thin Channel 5 Word Counter	Read/Write
03 002Ch	SYN_DLY	Sync Delay CH 4 & CH 5	Read/Write
03 0030h – 03 0FFC		Not Used	
03 1000h – 03 17FCh	GC4	Receiver Register Space Channel 4*	Read/Write
03 1800h – 03 1FFCh	GC5	Receiver Register Space Channel 5*	Read/Write
03 2000h – 03 FFFCh		Not Used	Read/Write
04 0000h	CSR_C6	Command/Status Register Channel 6	Read/Write
04 0004h	DWS_C6	Data Window Size Channel 6	Read/Write
04 0008h	RSKIP_C6	Receiver Data Skip Channel 6	Read/Write
04 000Ch	DATA_SEL6	Data Select Channel 6	Read/Write
04 0010h	CSR_C7	Command/Status Register Channel 7	Read/Write
04 0014h	DWS_C7	Data Window Size Channel 7	Read/Write
04 0018h	RSKIP_C7	Receiver Data Skip Channel 7	Read/Write
04 001Ch	DATA_SEL7	Data Select Channel 7	Read/Write
04 0020h	FIFOCNT	FIFO Word Counter	Read/Write
04 0024h	THIN_CNT6	Thin Channel 6 Word Counter	Read/Write
04 0028h	THIN_CNT7	Thin Channel 7 Word Counter	Read/Write
04 002Ch	SYN_DLY	Sync Delay CH 6 & CH 7	Read/Write
04 0030h – 04 0FFC		Not Used	
04 1000h – 04 17FCh	GC6	Receiver Register Space Channel 6*	Read/Write
04 1800h – 04 1FFCh	GC7	Receiver Register Space Channel 7*	Read/Write
04 2000h – 04 FFFCh		Not Used	Read/Write

***Not applicable when used as an AD board**

Table 6-14 Command / Status Register Channel

Abbreviation	Width	Address Offset	Mask	Attribute
CSR_C0 CSR_C1 CSR_C2 CSR_C3 CSR_C4 CSR_C5 CSR_C6 CSR_C7	32	01 0000h 01 0010h 02 0000h 02 0010h 03 0000h 03 0010h 04 0000h 04 0010h		Read/Write

Least Significant Word	
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	**Description**
	Mode Select 0h Raw AD 1h Counter 2h Receiver Data (packed) 3h Receiver Data (unpacked)
	Trigger Mode 00: Channel Disabled. 01: Trigger Mode: The Sync input or software sync will start acquisition and continue acquisition. Acquisition is stopped by the burst counter if the FREE RUN bit is low, or by writing the TRIGGER CLEAR bit if the FREE RUN bit is high. 1x: Gate Mode: The Sync input starts acquisition and continue acquisition. Acquisition is stopped by the Sync Input going inactive. The software sync and the FREE_RUN bit should not be used in this mode.
	Free Run 0: The Burst Counter controls the amount of data collected. 1: Data is collected continuously upon receipt of a sync.
	Not Used
	Trigger Clear (write only) Writing a 1 to this bit will stop the current acquisition cycle when the trigger mode it 01.
	FIFO Reset (write only) Writing a one to this bit resets this FIFO.
	Not Used

Table 6-14 Command / Status Register Channel (continued)

Abbreviation	Width	Address Offset	Mask	Attribute
CSR_C0 CSR_C1 CSR_C2 CSR_C3 CSR_C4 CSR_C5 CSR_C6 CSR_C7	32	01 0000h 01 0010h 02 0000h 02 0010h 03 0000h 03 0010h 04 0000h 04 0010h		Read/Write

Most Significant Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																SIA Sync Source Select Defines source for the SIA input to the Gray Chip 0h Disabled (default) 1h Software Global (from CSR register) 2h Software Local (see bit 20) 3h External Sync Input
																SIA Sync Type 0: Level that is released when the sync selected in SIA Sync Source Select register occurs. The level is enabled with the SIA Level Enable bit. 1: The SIA sync is issued to the Gray chip four clock cycles after the sync selected in SIA Sync Source Select Register occurs.
																SIA Level Enable Writing a 1 to this bit will enable the SIA sync when the SIA Sync Type register is a 0. A read back of a 1 will indicate that the SIA sync is enabled. This bit has no affect when the SIA Sync Type register is a 1.
																Software Local GC4016 SIA Sync Bit (write only) If selected by the SIA Sync Source Select bits, writing a 1h to this bit will issue a sync signal that can be driven out to this channels GC4016's SIA input.

Table 6-14 Command / Status Register Channel (continued)

Abbreviation	Width	Address Offset	Mask	Attribute
CSR_C0 CSR_C1 CSR_C2 CSR_C3 CSR_C4 CSR_C5 CSR_C6 CSR_C7	32	01 0000h 01 0010h 02 0000h 02 0010h 03 0000h 03 0010h 04 0000h 04 0010h		Read/Write

Most Significant Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																SIB Sync Source Select Defines source for the SIB input to the Gray Chip 0h Disabled (default) 1h Software Global (from CSR register) 2h Software Local (see bit 24) 3h External Sync Input
																SIB Sync Type 0: Level that is released when the sync selected in SIB Sync Source Select register occurs. The level is enabled with the SIB Level Enable bit. 1: The SIB sync is issued to the Gray chip four clock cycles after the sync selected in SIB Sync Source Select Register occurs.
																SIB Level Enable Writing a 1 to this bit will enable the SIB sync when the SIB Sync Type register is a 0. A read back of a 1 will indicate that the SIB sync is enabled. This bit has no affect when the SIB Sync Type register is a 1.
																Software Local GC4016 SIB Sync Bit (write only) If selected by the SIB Sync Source Select bits, writing a 1h to this bit will issue a sync signal that can be driven out to this channels GC4016's SIB input.
																Not Used
																Sync Delay Enable If enable is set to "0" then data collection starts when the Sync Pulse is received. If the enable bit is set to a "1" then data collection will be delayed based upon the count value loaded for SYN_DLY Counter (Table 6-20). 0 = Normal 1= Sync Delay Enabled
																Not Used

Table 6-15 Data Window Size Channel

Abbreviation	Width	Address Offset	Mask	Attribute
DWS_C0	32	01 0004h		Read/Write
DWS_C1		01 0014h		
DWS_C2		02 0004h		
DWS_C3		02 0014h		
DWS_C4		03 0004h		
DWS_C5		03 0014h		
DWS_C6		04 0004h		
DWS_C7		04 0014h		

Least Significant Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Burst Count Value: This is the acquisition sample count – the number of words that are acquired when a trigger is received. The value written should be 1 less than the desired total number of words to be collected. If the user is in the "Raw Data to Accumulator" mode with an accumulate of 1, then the value written should be 2 less than the desired total number of words to be collected.

Most Significant Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Burst Count Value (Continued) Note: Bit 17 can only be used for setting the DWS when the FIFO Ping-Pong mode is used and the FIFO is a 128K device.
																Not Used

Table 6-16 Receiver Data Skip Channel

Abbreviation	Width	Address Offset	Mask	Attribute
RSKIP_C0 RSKIP_C1 RSKIP_C2 RSKIP_C3 RSKIP_C4 RSKIP_C5 RSKIP_C6 RSKIP_C7	32	01 0008h 01 0018h 02 0008h 02 0018h 03 0008h 03 0018h 04 0008h 04 0018h		Read/Write

Least Significant Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																Receiver Data Skip Counter: The Receiver Data Skip function is only valid when Receiver Data is selected by bits 0 & 1 of channel CSR. When Receiver Data is selected, the value loaded into Receiver Skip Counter defines how many valid data samples are skipped prior to storing receiver data in the FIFO.

Most Significant Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

Table 6-17 Data Select

Abbreviation	Width	Address Offset	Mask	Attribute
DATA_SEL 0 DATA_SEL 1 DATA_SEL 2 DATA_SEL 3 DATA_SEL 4 DATA_SEL 5 DATA_SEL 6 DATA_SEL 7	32	01 000Ch 01 001Ch 02 000Ch 02 001Ch 03 000Ch 03 001Ch 04 000Ch 04 001Ch		Read/Write

Least Significant Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																When RAW A/D is selected by bits 0 & 1 of the CSR (Table 6-14), then the following modes are available: **Normal Mode** 0h = Normal Mode **16 Bit Thinning** 1h =16 bit Thinning Setting this bit selects the raw A/D data to be thinned by the selection entered into THIN_CNT word counter. **8 Bit Packing** 2h = Packing Mode Setting this bit selects the raw A/D data to be truncated and packed 4 samples to a 32 bit word.
																FIFO Ping Pong **This function has been incorporated for 8 channel boards. The function allows for FIFO memory space that would normally be used for 2 channels to be used by the lower channel of each pair (0 &1, 2 & 3, 4 & 5, 6 & 7).** Writing this bit to a 1 will enable Single Channel (Ping Pong) in all modes of operation. Reference Table 6-18.
																Not Used

Most Significant Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

Table 6-18 FIFO Word Counter

Abbreviation	Width	Address Offset	Mask	Attribute
FIFOCNT0 FIFOCNT2 FIFOCNT4 FIFOCNT6	32	01 0020h 02 0020h 03 0020h 04 0020h		Read/Write

Least Significant Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																FIFO Counter **When the enable bit is set (Reference Table 6-17) to a 1 (Enable Single Channel) only the data from the lower channel, of the channel pair, will collect data. Loading the FIFO Counter to the desired value will control how much data is written to the lower channel FIFO before switching to the other FIFO.** Write this counter 1 less than the intended count. 1FFFE h = Max Count

Most Significant Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																FIFO Counter (continued) **Not Used**

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Table 6-19 THIN_CNT Word Counter

Abbreviation	Width	Address Offset	Mask	Attribute
THIN_CN0 THIN_CN1 THIN_CN2 THIN_CN3 THIN_CN4 THIN_CN5 THIN_CN6 THIN_CN7	32	01 0024h 01 0028h 02 0024h 02 0028h 03 0024h 03 0028h 04 0024h 04 0028h		Read/Write

Least Significant Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																When "16 Bit Thinning" is enabled (Reference Table 6-17), the value loaded into "Thin Count Counter" will control the thinning rate of the Raw A/D data. See Data Format in chapter 5. **Thin Data Counter** 1h = Thin X2 3h = Thin X4 7h = Thin X8 Eh= Thin X16 1Eh= Thin X32 3Eh = Thin X64
																Not Used

Most Significant Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

Table 6-20 Sync_Delay Counter

Abbreviation	Width	Address Offset	Mask	Attribute
Syn_Dly_Ch 0 & 1	32	01 002Ch		Read/Write
Syn_Dly_Ch 2& 3	32	02 002Ch		Read/Write
Syn_Dly_Ch 4 & 5	32	03 002Ch		Read/Write
Syn_Dly_Ch 6 & 7	32	04 002Ch		Read/Write

Least Significant Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																When " Sync Delay Enable " is enabled (Reference Table 6-11), the value loaded into " Syn_Dly Counter " will control the delay from received Sync to the start of data collection. **Syn Dly Counter** • Minimum Count Value =1 • Delay = # of counts X Clock Period • Example: Count of 50h and Clock of 80 Mhz Delay = 80 X 12.5 ns = 1µs **In the above example there will be a 1µs delay from receiving Sync to the start of data collection.**
																Not Used

Most Significant Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Description
																Not Used

Receivers Configuration Registers

The following tables show register maps for receiver channels A, B, C, and D, resampler coefficients, and resampler control and ratios/output data and control. For the definitions and use of each register, refer to the Graychip GC4016 Data Sheet.

Table 6-21 Channel A Control Register Map

ADDRESS OFFSET	D31-D24	D23-D16	D15-D8	D7-D0
000	CFIR-H1(MSB)	H1(LSB)	H0(MSB)	H0(LSB)
004	H3(MSB)	H3(LSB)	H2(MSB)	H2(LSB)
008	H5(MSB)	H5(LSB)	H4(MSB)	H4(LSB)
00C	H7(MSB)	H7(LSB)	H6(MSB)	H6(LSB)
010	H9(MSB)	H9(LSB)	H8(MSB)	H8(LSB)
014			H10(MSB)	H10(LSB)
018				
01C				
020	PFIR-H1(MSB)	H1(LSB)	H0(MSB)	H0(LSB)
024	H3(MSB)	H3(LSB)	H2(MSB)	H2(LSB)
028	H5(MSB)	H5(LSB)	H4(MSB)	H4(LSB)
02C	H7(MSB)	H7(LSB)	H6(MSB)	H6(LSB)
030	H9(MSB)	H9(LSB)	H8(MSB)	H8(LSB)
034	H11(MSB)	H11(LSB)	H10(MSB)	H10(LSB)
038	H13(MSB)	H13(LSB)	H12(MSB)	H12(LSB)
03C	H15(MSB)	H15(LSB)	H14(MSB)	H14(LSB)
040	H17(MSB)	H17(LSB)	H16(MSB)	H16(LSB)
044	H19(MSB)	H19(LSB)	H18(MSB)	H18(LSB)
048	H21(MSB)	H21(LSB)	H20(MSB)	H20(LSB)
04C	H23(MSB)	H23(LSB)	H22(MSB)	H22(LSB)
050	H25(MSB)	H25(LSB)	H24(MSB)	H24(LSB)
054	H27(MSB)	H27(LSB)	H26(MSB)	H26(LSB)
058	H29(MSB)	H29(LSB)	H28(MSB)	H28(LSB)
05C	H31(MSB)	H31(LSB)	H30(MSB)	H30(LSB)
060	FREQ-B1	FREQ-B0(LSB)	PHASE(MSB)	PHASE(LSB)

Table 6-21 Channel A Control Register Map (continued)

ADDRESS OFFSET	D31-D24	D23-D16	D15-D8	D7-D0
064			FREQ-B3(MSB)	FREQ-B2
068				
06C				
070	ZERO PAD MODE CTRL	NCO SYNC	FREQ SYNC	CH RESET
074	CIC SCALE	DEC RATIO (MSB)	DEC RATIO (LSB)	DEC & FLUSH SYNC
078	INPUT	PFIR	CFIR	SPLIT IQ
07C	FINE GAIN (MSB)	FINE GAIN (LSB)	PEAK COUNT	PEAK CTRL

Table 6-22 Channel B Control Register Map

ADDRESS OFFSET	D31-D24	D23-D16	D15-D8	D7-D0
080	CFIR-H1(MSB)	H1(LSB)	H0(MSB)	H0(LSB)
084	H3(MSB)	H3(LSB)	H2(MSB)	H2(LSB)
088	H5(MSB)	H5(LSB)	H4(MSB)	H4(LSB)
08C	H7(MSB)	H7(LSB)	H6(MSB)	H6(LSB)
090	H9(MSB)	H9(LSB)	H8(MSB)	H8(LSB)
094			H10(MSB)	H10(LSB)
098				
09C				
0A0	PFIR-H1(MSB)	H1(LSB)	H0(MSB)	H0(LSB)
0A4	H3(MSB)	H3(LSB)	H2(MSB)	H2(LSB)
0A8	H5(MSB)	H5(LSB)	H4(MSB)	H4(LSB)
0AC	H7(MSB)	H7(LSB)	H6(MSB)	H6(LSB)
0B0	H9(MSB)	H9(LSB)	H8(MSB)	H8(LSB)
0B4	H11(MSB)	H11(LSB)	H10(MSB)	H10(LSB)
0B8	H13(MSB)	H13(LSB)	H12(MSB)	H12(LSB)
0BC	H15(MSB)	H15(LSB)	H14(MSB)	H14(LSB)
0C0	H17(MSB)	H17(LSB)	H16(MSB)	H16(LSB)
0C4	H19(MSB)	H19(LSB)	H18(MSB)	H18(LSB)
0C8	H21(MSB)	H21(LSB)	H20(MSB)	H20(LSB)
0CC	H23(MSB)	H23(LSB)	H22(MSB)	H22(LSB)
0D0	H25(MSB)	H25(LSB)	H24(MSB)	H24(LSB)
0D4	H27(MSB)	H27(LSB)	H26(MSB)	H26(LSB)
0D8	H29(MSB)	H29(LSB)	H28(MSB)	H28(LSB)
0DC	H31(MSB)	H31(LSB)	H30(MSB)	H30(LSB)
0E0	FREQ-B1	FREQ-B0(LSB)	PHASE(MSB)	PHASE(LSB)
0E4			FREQ-B3(MSB)	FREQ-B2
0E8				
0EC				

Table 6-22 Channel B Control Register Map (continued)

ADDRESS OFFSET	D31-D24	D23-D16	D15-D8	D7-D0
0F0	ZERO PAD MODE CTRL	NCO SYNC	FREQ SYNC	CH RESET
0F4	CIC SCALE	DEC RATIO (MSB)	DEC RATIO (LSB)	DEC & FLUSH SYNC
0F8	INPUT	PFIR	CFIR	SPLIT IQ
0FC	FINE GAIN (MSB)	FINE GAIN (LSB)	PEAK COUNT	PEAK CTRL

Table 6-23 Channel C Control Register Map

ADDRESS OFFSET	D31-D24	D23-D16	D15-D8	D7-D0
100	CFIR-H1(MSB)	H1(LSB)	H0(MSB)	H0(LSB)
104	H3(MSB)	H3(LSB)	H2(MSB)	H2(LSB)
108	H5(MSB)	H5(LSB)	H4(MSB)	H4(LSB)
10C	H7(MSB)	H7(LSB)	H6(MSB)	H6(LSB)
110	H9(MSB)	H9(LSB)	H8(MSB)	H8(LSB)
114			H10(MSB)	H10(LSB)
118				
11C				
120	PFIR-H1(MSB)	H1(LSB)	H0(MSB)	H0(LSB)
124	H3(MSB)	H3(LSB)	H2(MSB)	H2(LSB)
128	H5(MSB)	H5(LSB)	H4(MSB)	H4(LSB)
12C	H7(MSB)	H7(LSB)	H6(MSB)	H6(LSB)
130	H9(MSB)	H9(LSB)	H8(MSB)	H8(LSB)
134	H11(MSB)	H11(LSB)	H10(MSB)	H10(LSB)
138	H13(MSB)	H13(LSB)	H12(MSB)	H12(LSB)
13C	H15(MSB)	H15(LSB)	H14(MSB)	H14(LSB)
140	H17(MSB)	H17(LSB)	H16(MSB)	H16(LSB)
144	H19(MSB)	H19(LSB)	H18(MSB)	H18(LSB)
148	H21(MSB)	H21(LSB)	H20(MSB)	H20(LSB)
14C	H23(MSB)	H23(LSB)	H22(MSB)	H22(LSB)
150	H25(MSB)	H25(LSB)	H24(MSB)	H24(LSB)
154	H27(MSB)	H27(LSB)	H26(MSB)	H26(LSB)
158	H29(MSB)	H29(LSB)	H28(MSB)	H28(LSB)
15C	H31(MSB)	H31(LSB)	H30(MSB)	H30(LSB)
160	FREQ-B1	FREQ-B0(LSB)	PHASE(MSB)	PHASE(LSB)
164			FREQ-B3(MSB)	FREQ-B2
168				
16C				

Table 6-23 Channel C Control Register Map (continued)

ADDRESS OFFSET	D31-D24	D23-D16	D15-D8	D7-D0
170	ZERO PAD MODE CTRL	NCO SYNC	FREQ SYNC	CH RESET
174	CIC SCALE	DEC RATIO (MSB)	DEC RATIO (LSB)	DEC & FLUSH SYNC
178	INPUT	PFIR	CFIR	SPLIT IQ
17C	FINE GAIN (MSB)	FINE GAIN (LSB)	PEAK COUNT	PEAK CTRL

Table 6-24 Channel D Control Register Map

ADDRESS OFFSET	D31-D24	D23-D16	D15-D8	D7-D0
180	CFIR-H1(MSB)	H1(LSB)	H0(MSB)	H0(LSB)
184	H3(MSB)	H3(LSB)	H2(MSB)	H2(LSB)
188	H5(MSB)	H5(LSB)	H4(MSB)	H4(LSB)
18C	H7(MSB)	H7(LSB)	H6(MSB)	H6(LSB)
190	H9(MSB)	H9(LSB)	H8(MSB)	H8(LSB)
194			H10(MSB)	H10(LSB)
198				
19C				
1A0	PFIR-H1(MSB)	H1(LSB)	H0(MSB)	H0(LSB)
1A4	H3(MSB)	H3(LSB)	H2(MSB)	H2(LSB)
1A8	H5(MSB)	H5(LSB)	H4(MSB)	H4(LSB)
1AC	H7(MSB)	H7(LSB)	H6(MSB)	H6(LSB)
1B0	H9(MSB)	H9(LSB)	H8(MSB)	H8(LSB)
1B4	H11(MSB)	H11(LSB)	H10(MSB)	H10(LSB)
1B8	H13(MSB)	H13(LSB)	H12(MSB)	H12(LSB)
1BC	H15(MSB)	H15(LSB)	H14(MSB)	H14(LSB)
1C0	H17(MSB)	H17(LSB)	H16(MSB)	H16(LSB)
1C4	H19(MSB)	H19(LSB)	H18(MSB)	H18(LSB)
1C8	H21(MSB)	H21(LSB)	H20(MSB)	H20(LSB)
1CC	H23(MSB)	H23(LSB)	H22(MSB)	H22(LSB)
1D0	H25(MSB)	H25(LSB)	H24(MSB)	H24(LSB)
1D4	H27(MSB)	H27(LSB)	H26(MSB)	H26(LSB)
1D8	H29(MSB)	H29(LSB)	H28(MSB)	H28(LSB)
1DC	H31(MSB)	H31(LSB)	H30(MSB)	H30(LSB)
1E0	FREQ-B1	FREQ-B0(LSB)	PHASE(MSB)	PHASE(LSB)
1E4			FREQ-B3(MSB)	FREQ-B2
1E8				
1EC				

Table 6-24 Channel D Control Register Map (continued)

ADDRESS OFFSET	D31-D24	D23-D16	D15-D8	D7-D0
1F0	ZERO PAD MODE CTRL	NCO SYNC	FREQ SYNC	CH RESET
1F4	CIC SCALE	DEC RATIO (MSB)	DEC RATIO (LSB)	DEC & FLUSH SYNC
1F8	INPUT	PFIR	CFIR	SPLIT IQ
1FC	FINE GAIN (MSB)	FINE GAIN (LSB)	PEAK COUNT	PEAK CTRL

Table 6-25 Resampler Coefficients Register Map

ADDRESS OFFSET	D31-D24 (D27-D24 USED)	D23-D16	D15-D8 (D11-D8 USED)	D7-D0
200	H1(MSB)	H1(LSB)	H0(MSB)	H0(LSB)
204	H3(MSB)	H3(LSB)	H2(MSB)	H2(LSB)
208	H5(MSB)	H5(LSB)	H4(MSB)	H4(LSB)
20C	H7(MSB)	H7(LSB)	H6(MSB)	H6(LSB)
210	H9(MSB)	H9(LSB)	H8(MSB)	H8(LSB)
214	H11(MSB)	H11(LSB)	H10(MSB)	H10(LSB)
218	H13(MSB)	H13(LSB)	H12(MSB)	H12(LSB)
21C	H15(MSB)	H15(LSB)	H14(MSB)	H14(LSB)
220	H17(MSB)	H17(LSB)	H16(MSB)	H16(LSB)
224	H19(MSB)	H19(LSB)	H18(MSB)	H18(LSB)
228	H21(MSB)	H21(LSB)	H20(MSB)	H20(LSB)
22C	H23(MSB)	H23(LSB)	H22(MSB)	H22(LSB)
230	H25(MSB)	H25(LSB)	H24(MSB)	H24(LSB)
234	H27(MSB)	H27(LSB)	H26(MSB)	H26(LSB)
238	H29(MSB)	H29(LSB)	H28(MSB)	H28(LSB)
23C	H31(MSB)	H31(LSB)	H30(MSB)	H30(LSB)
240	H33(MSB)	H33(LSB)	H32(MSB)	H32(LSB)
244	H35(MSB)	H35(LSB)	H34(MSB)	H34(LSB)
248	H37(MSB)	H37(LSB)	H36(MSB)	H36(LSB)
24C	H39(MSB)	H39(LSB)	H38(MSB)	H38(LSB)
250	H41(MSB)	H41(LSB)	H40(MSB)	H40(LSB)
254	H43(MSB)	H43(LSB)	H42(MSB)	H42(LSB)
258	H45(MSB)	H45(LSB)	H44(MSB)	H44(LSB)
25C	H47(MSB)	H47(LSB)	H46(MSB)	H46(LSB)
260	H49(MSB)	H49(LSB)	H48(MSB)	H48(LSB)
264	H51(MSB)	H51(LSB)	H50(MSB)	H50(LSB)
268	H53(MSB)	H53(LSB)	H52(MSB)	H52(LSB)
26C	H55(MSB)	H55(LSB)	H54(MSB)	H54(LSB)

Table 6-25 Resampler Coefficients Register Map (continued)

ADDRESS OFFSET	D31-D24 (D27-D24 USED)	D23-D16	D15-D8 (D11-D8 USED)	D7-D0
270	H57(MSB)	H57(LSB)	H56(MSB)	H56(LSB)
274	H59(MSB)	H59(LSB)	H58(MSB)	H58(LSB)
278	H61(MSB)	H61(LSB)	H60(MSB)	H60(LSB)
27C	H63(MSB)	H63(LSB)	H62(MSB)	H62(LSB)
280	H65(MSB)	H65(LSB)	H64 (MSB)	H64(LSB)
284	H67(MSB)	H67(LSB)	H66 (MSB)	H66(LSB)
288	H69(MSB)	H69(LSB)	H68(MSB)	H68(LSB)
28C	H71(MSB)	H71(LSB)	H70(MSB)	H70(LSB)
290	H73(MSB)	H73(LSB)	H72(MSB)	H72(LSB)
294	H75(MSB)	H75(LSB)	H74(MSB)	H74(LSB)
298	H77(MSB)	H77(LSB)	H76(MSB)	H76(LSB)
29C	H79(MSB)	H79(LSB)	H78(MSB)	H78(LSB)
2A0	H81(MSB)	H81(LSB)	H80(MSB)	H80(LSB)
2A4	H83(MSB)	H83(LSB)	H82(MSB)	H82(LSB)
2A8	H85(MSB)	H85(LSB)	H84(MSB)	H84(LSB)
2AC	H87(MSB)	H87(LSB)	H86(MSB)	H86(LSB)
2B0	H89(MSB)	H89(LSB)	H88(MSB)	H88(LSB)
2B4	H91(MSB)	H91(LSB)	H90(MSB)	H90(LSB)
2B8	H93(MSB)	H93(LSB)	H92(MSB)	H92(LSB)
2BC	H95(MSB)	H95(LSB)	H94(MSB)	H94(LSB)
2C0	H97(MSB)	H97(LSB)	H96(MSB)	H96(LSB)
2C4	H99(MSB)	H99(LSB)	H98(MSB)	H98(LSB)
2C8	H101(MSB)	H101(LSB)	H100(MSB)	H100(LSB)
2CC	H103(MSB)	H103(LSB)	H102(MSB)	H102(LSB)
2D0	H105(MSB)	H105(LSB)	H104(MSB)	H104(LSB)
2D4	H107(MSB)	H107(LSB)	H106(MSB)	H106(LSB)
2D8	H109(MSB)	H109(LSB)	H108(MSB)	H108(LSB)
2DC	H111(MSB)	H111(LSB)	H110(MSB)	H110(LSB)

Table 6-25 Resampler Coefficients Register Map (continued)

ADDRESS OFFSET	D31-D24 (D27-D24 USED)	D23-D16	D15-D8 (D11-D8 USED)	D7-D0
2E0	H113(MSB)	H113(LSB)	H112(MSB)	H112(LSB)
2E4	H115(MSB)	H115(LSB)	H114(MSB)	H114(LSB)
2E8	H117(MSB)	H117(LSB)	H116(MSB)	H116(LSB)
2EC	H119(MSB)	H119(LSB)	H118(MSB)	H118(LSB)
2F0	H121(MSB)	H121(LSB)	H120(MSB)	H120(LSB)
2F4	H123(MSB)	H123(LSB)	H122(MSB)	H122(LSB)
2F8	H125(MSB)	H125(LSB)	H124(MSB)	H124(LSB)
2FC	H127(MSB)	H127(LSB)	H126(MSB)	H126(LSB)
300	H129(MSB)	H129(LSB)	H128(MSB)	H128(LSB)
304	H131(MSB)	H131(LSB)	H130(MSB)	H130(LSB)
308	H133(MSB)	H133(LSB)	H132(MSB)	H132(LSB)
30C	H135(MSB)	H135(LSB)	H134(MSB)	H134(LSB)
310	H137(MSB)	H137(LSB)	H136(MSB)	H136(LSB)
314	H139(MSB)	H139(LSB)	H138(MSB)	H138(LSB)
318	H141(MSB)	H141(LSB)	H140(MSB)	H140(LSB)
31C	H143(MSB)	H143(LSB)	H142(MSB)	H142(LSB)
320	H145(MSB)	H145(LSB)	H144(MSB)	H144(LSB)
324	H147(MSB)	H147(LSB)	H146(MSB)	H146(LSB)
328	H149(MSB)	H149(LSB)	H148(MSB)	H148(LSB)
32C	H151(MSB)	H151(LSB)	H150(MSB)	H150(LSB)
330	H153(MSB)	H153(LSB)	H152(MSB)	H152(LSB)
334	H155(MSB)	H155(LSB)	H154(MSB)	H154(LSB)
338	H157(MSB)	H157(LSB)	H156(MSB)	H156(LSB)
33C	H159(MSB)	H159(LSB)	H158(MSB)	H158(LSB)
340	H161(MSB)	H161(LSB)	H160(MSB)	H160(LSB)
344	H163(MSB)	H163(LSB)	H162(MSB)	H162(LSB)
348	H165(MSB)	H165(LSB)	H164(MSB)	H164(LSB)
34C	H167(MSB)	H167(LSB)	H166(MSB)	H166(LSB)

Table 6-25 Resampler Coefficients Register Map (continued)

ADDRESS OFFSET	D31-D24 (D27-D24 USED)	D23-D16	D15-D8 (D11-D8 USED)	D7-D0
350	H169(MSB)	H169(LSB)	H168(MSB)	H168(LSB)
354	H171(MSB)	H171(LSB)	H170(MSB)	H170(LSB)
358	H173(MSB)	H173(LSB)	H172(MSB)	H172(LSB)
35C	H175(MSB)	H175(LSB)	H174(MSB)	H174(LSB)
360	H177(MSB)	H177(LSB)	H176(MSB)	H176(LSB)
364	H179(MSB)	H179(LSB)	H178(MSB)	H178(LSB)
368	H181(MSB)	H181(LSB)	H180(MSB)	H180(LSB)
36C	H183(MSB)	H183(LSB)	H182(MSB)	H182(LSB)
370	H185(MSB)	H185(LSB)	H184(MSB)	H184(LSB)
374	H187(MSB)	H187(LSB)	H186(MSB)	H186(LSB)
378	H189(MSB)	H189(LSB)	H188(MSB)	H188(LSB)
37C	H191(MSB)	H191(LSB)	H190(MSB)	H190(LSB)
380	H193(MSB)	H193(LSB)	H192(MSB)	H192(LSB)
384	H195(MSB)	H195(LSB)	H194(MSB)	H194(LSB)
388	H197(MSB)	H197(LSB)	H196(MSB)	H196(LSB)
38C	H199(MSB)	H199(LSB)	H198(MSB)	H198(LSB)
390	H201(MSB)	H201(LSB)	H200(MSB)	H200(LSB)
394	H203(MSB)	H203(LSB)	H202(MSB)	H202(LSB)
398	H205(MSB)	H205(LSB)	H204(MSB)	H204(LSB)
39C	H207(MSB)	H207(LSB)	H206(MSB)	H206(LSB)
3A0	H209(MSB)	H209(LSB)	H208(MSB)	H208(LSB)
3A4	H211(MSB)	H211(LSB)	H210(MSB)	H210(LSB)
3A8	H213(MSB)	H213(LSB)	H212(MSB)	H212(LSB)
3AC	H215(MSB)	H215(LSB)	H214(MSB)	H214(LSB)
3B0	H217(MSB)	H217(LSB)	H216(MSB)	H216(LSB)
3B4	H219(MSB)	H219(LSB)	H218(MSB)	H218(LSB)
3B8	H221(MSB)	H221(LSB)	H220(MSB)	H220(LSB)
3BC	H223(MSB)	H223(LSB)	H222(MSB)	H222(LSB)

Table 6-25 Resampler Coefficients Register Map (continued)

ADDRESS OFFSET	D31-D24 (D27-D24 USED)	D23-D16	D15-D8 (D11-D8 USED)	D7-D0
3C0	H225(MSB)	H225(LSB)	H224(MSB)	H224(LSB)
3C4	H227(MSB)	H227(LSB)	H226(MSB)	H226(LSB)
3C8	H229(MSB)	H229(LSB)	H228(MSB)	H228(LSB)
3CC	H231(MSB)	H231(LSB)	H230(MSB)	H230(LSB)
3D0	H233(MSB)	H233(LSB)	H232(MSB)	H232(LSB)
3D4	H235(MSB)	H235(LSB)	H234(MSB)	H234(LSB)
3D8	H237(MSB)	H237(LSB)	H236(MSB)	H236(LSB)
3DC	H239(MSB)	H239(LSB)	H238(MSB)	H238(LSB)
3E0	H241(MSB)	H241(LSB)	H240(MSB)	H240(LSB)
3E4	H243(MSB)	H243(LSB)	H242(MSB)	H242(LSB)
3E8	H245(MSB)	H245(LSB)	H244(MSB)	H244(LSB)
3EC	H247(MSB)	H247(LSB)	H246(MSB)	H246(LSB)
3F0	H249(MSB)	H249(LSB)	H248(MSB)	H248(LSB)
3F4	H251(MSB)	H251(LSB)	H250(MSB)	H250(LSB)
3F8	H253(MSB)	H253(LSB)	H252(MSB)	H252(LSB)
3FC	H255(MSB)	H255(LSB)	H254(MSB)	H254(LSB)

Table 6-26 Resampler Control and Ratios/Output Data and Control Register Map

ADDRESS OFFSET	D31-D24	D23-D16	D15-D8	D7-D0
400	Final Shift	Filter Select	N-multiplies	N-Channels Out
404		Resampler Clock Divide	Add-To	Channel Map
408				
40C				
410	Ratio_0-B4 (MSB)	Ratio_0-B3	Ratio_0–B2	Ratio_0–B1 (LSB)
414	Ratio_1-B4 (MSB)	Ratio_1-B3	Ratio_1–B2	Ratio_1–B1 (LSB)
418	Ratio_2-B4 (MSB)	Ratio_2-B3	Ratio_2–B2	Ratio_2–B1 (LSB)
41C	Ratio_3-B4 (MSB)	Ratio_3-B3	Ratio_3–B2	Ratio_3–B1 (LSB)
420	Channel Output	Channel Output	Channel Output	Channel Output
424	Channel Output	Channel Output	Channel Output	Channel Output
428	Channel Output	Channel Output	Channel Output	Channel Output
42C	Channel Output	Channel Output	Channel Output	Channel Output
430	Channel Output	Channel Output	Channel Output	Channel Output
434	Channel Output	Channel Output	Channel Output	Channel Output
438	Channel Output	Channel Output	Channel Output	Channel Output
43C	Channel Output	Channel Output	Channel Output	Channel Output
440	Checksum	Page	Status	Global Reset
444	Counter (MSB)	Counter (LSB)	Count Sync	General Sync
448				
44C				
450	Output Frame Control	Output Mode	Output Format	Tristate Controls
454	Output Tag A	Serial Mux Control	Output Clock Control	Output Word Sizes
458	Mask Revision	Output Tag D	Output Tag C	Output Tag B

GC4016 Registers

The following tables show the GC4016 register bit fields for register maps described in the "Receivers Configuration Registers" section in this chapter. For a complete description of these registers, refer to the latest Graychip GC4016 Data Sheet.

Table 6-27 Global Control Registers

Register Name	D7	D6	D5	D4	D3	D2	D1	D0
Global Reset	GLOBAL _RESET	OUT_BLK _RESET	PAD_RESET	RESAMPLER_ RESET	EDGE _WRITE	CK_2X_EN	CK_2X_TEST	CK_LOSS _DETECT
Status	ZERO			CHECK _DONE	RES_QOV	RES_IOV	MISSED	READY
Page	PAGE							A3
Check-sum	CHECKSUM[0:7]							
General Syncs	LVDS	4_BIT _ADDRES S	OUTPUT_SYNC			DIAG_SYNC		
Count Sync	ONE_SHOT	UNUSED	COUNT _TEST	COUNTER_SYNC			DIAG_SOURCE	
Counter Byte 0	CNT[0:7]							
Counter Byte 1	CNT[8:15]							

Table 6-28 Output Control Registers

Register Name	D7	D6	D5	D4	D3	D2	D1	D0
Tristate Controls	EN_PAR	EN_P3	EN_P2	EN_P1	EN_P0	EN_SFS	EN_RDY	EN_SCK
Output Format	OUT_BLK_SYNC			RDY_WIDTH	TAG_EN	INF_SFS	INV_RDY	INV_SCK
Output Control	REVERSE_IQ	OUTPUT_MODE		REAL_ONLY	MASTER	PARALLEL	NIBBLE	LINK
Output Frame Control	SFS_MODE		FRAME_LENGTH					
Output Word Sizes	BLOCK_SIZE		BITS_PER_WORD			WORDS_PER_FRAME		
Output Clock Control	OUTPUT_ORDER		NSERIAL		SCK_RATE			
Serial Mux Control	SMUX_3		SMUX_2		SMUX_1		SMUX_0	
Output Tag A	TAG_AQ				TAG_AI			
Output Tag B	TAG_BQ				TAG_BI			
Output Tag C	TAG_CQ				TAG_CI			
Output Tag D	TAG_DQ				TAG_DI			
Mask Revision	REVISION							

Table 6-29 Channel Frequency Registers

Register Name	D7	D6	D5	D4	D3	D2	D1	D0
Phase Byte 0	PHASE[0:7]							
Phase Byte 1	PHASE[8:15]							
Frequency Byte 0	FREQ[0:7]							
Frequency Byte 1	FREQ[8:15]							
Frequency Byte 2	FREQ[16:23]							
Frequency Byte 3	FREQ[24:31]							

Table 6-30 Channel Control Registers

Register Name	D7	D6	D5	D4	D3	D2	D1	D0
Channel Reset	CH_RESET	UNUSED			USE_SHIFT	SHIFT		
Frequency Sync	UNUSED	FREQ_SYNC			UNUSED	PHASE_SYNC		
NCO Sync	UNUSED	DITHER_SYNC			UNUSED	NCO_SYNC		
Blank	ZPAD_EN	ZPAD_SYNC			NZEROES			
Dec Sync	UNUSED	FLUSH_SYNC			UNUSED	DEC_SYNC		
Decimation Ratio Byte 0	DEC[0:7]							
Decimation Ratio Byte 1	UNUSED	GAIN_SYNC			DEC[8:11]			
CIC Scale	UNUSED	MIX20B	BIG_SCALE		SCALE			
SplitIQ	UNUSED	QONLY	IONLY	SPLITIQ	NEG_CTRL			
CFIR	TEST	COARSE			UNUSED	IDLY_CFIR	QDLY_CFIR	NO_SYM_CFIR
PFIR	UNUSED		PEAK_SELECT			IDLY_PFIR	QDLY_PFIR	NO_SYM_PFIR
Input	MSB_POL	UNUSED	IN_FMT		AB_SEL	INPUT_SEL		
Peak Control	UNUSED		PEAK_MODE	PEAK_THRESH		PEAK_SYNC		
Peak Count	PEAK_COUNT							
Fine Gain Byte 0	FINE_GAIN[0:7]							
Fine Gain Byte 1	UNUSED	FINE_GAIN[8:13]						

Table 6-31 Resampler Control Registers

Register Name	D7	D6	D5	D4	D3	D2	D1	D0
N-Channels Out	UNUSED				NF = NFILTER-1		NC = NCHAN-1	
N-Multiplies	UNUSED	NO_SYM _RES	NM = NMULT-1					
Filter Select	FILTER_SEL_3		FILTER_SEL_2		FILTER_SEL_1		FILTER_SEL_0	
Final Shift	UNUSED		ROUND		FINAL_SHIFT			
Channel Map	CHAN_MAP_D		CHAN_MAP_C		CHAN_MAP_B		CHAN_MAP_A	
Add To	UNUSED				UNUSED MUST=0	ADD_C TO_D	ADD_B TO_C	ADD_A TO_B
Clock Divide	RES_CLK_DIV							

Table 6-32 Resample Ratio Registers

Register Name	D7	D6	D5	D4	D3	D2	D1	D0
Ratio_0 Byte0	RATIO_0_B0							
Ratio_0 Byte1	RATIO_0_B1							
Ratio_0 Byte2	RATIO_0_B2							
Ratio_0 Byte3	RATIO_0_B3							
Ratio_1 Byte0	RATIO_1_B0							
Ratio_1 Byte1	RATIO_1_B1							
Ratio_1 Byte2	RATIO_1_B2							
Ratio_1 Byte3	RATIO_1_B3							
Ratio_2 Byte0	RATIO_2_B0							
Ratio_2 Byte1	RATIO_2_B1							
Ratio_2 Byte2	RATIO_2_B2							
Ratio_2 Byte3	RATIO_2_B3							
Ratio_3 Byte0	RATIO_3_B0							
Ratio_3 Byte1	RATIO_3_B1							
Ratio_3 Byte2	RATIO_3_B2							
Ratio_3 Byte3	RATIO_3_B3							

Table 6-33 GC4016 Required Register Configuration

GC4016 Register	Register Value (Binary)	Description
Global Reset	XXXX 1XXX	Edge Write must be ENABLED.
General Syncs	00XX XXXX	LVDS must be DISABLED. 4 Bit Address Mode must be DISABLED.
Tristate Controls	1111 1111 (FFh)	All Control Signal Outputs must be ENABLED.
Output Format	XXX0 1001	RDY Width must be ZERO. Tags must be ENABLED. SFS must be NON-INVERTED. RDY Must be NON-INVERTED. SCK must be INVERTED.
Output Mode	X11X 1100	Output Mode must be PARALLEL. Master must be ENABLED. Parallel Mode must be ENABLED. Nibble Mode must be DISABLED. LINK Mode must be DISABLED.
Output Frame Control	11XX XXXX	SFS Mode must be 3: SFS = Data VALID, RDY = Frame Sync
Output Word Size	XX10 1XXX	Bits Per Word must be 24 (Program value = 5).
Output Clock Control	XX00 0001	NSERIAL must be 0. SCK Divide must be 2 (Program value = 1).
Output Tag A	0001 0000 (10h)	I Tag must be 0. Q Tag must be 1.
Output Tag B	0011 0010 (32h)	I Tag must be 2. Q Tag must be 3.
Output Tag C	0101 0100 (54h)	I Tag must be 4. Q Tag must be 5.
Output Tag D	0111 0110 (76h)	I Tag must be 6. Q Tag must be 7.